

Version 0A
08/09/2005 Update

CPU:

Intel LGA775 Processor

System Chipset:

SIS 656 + SiS 965L

On Board Chipset:

LPC Super I/O -- W83697HF
LAN PHY -- VT6103
IEEE1394 -- VT6307
AC97 CODEC -- RealTek ALC850

CLOCK Chip :

ICS953401+ Buffer ICS9P932

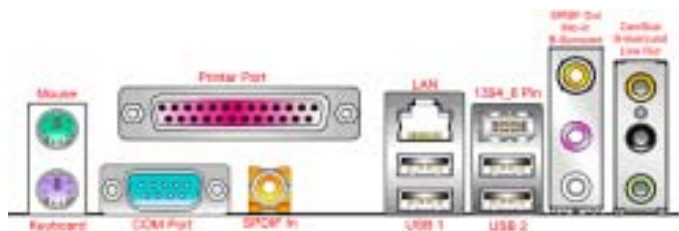
Main Memory:

DDR2 DIMM Slot *4

Expansion Slots:


PCI EXPRESS x16 Slot *1
PCI EXPRESS x1 Slot *1
PCI2.2 Slot *2

PWM:

INTERSIL ISL6565ACV

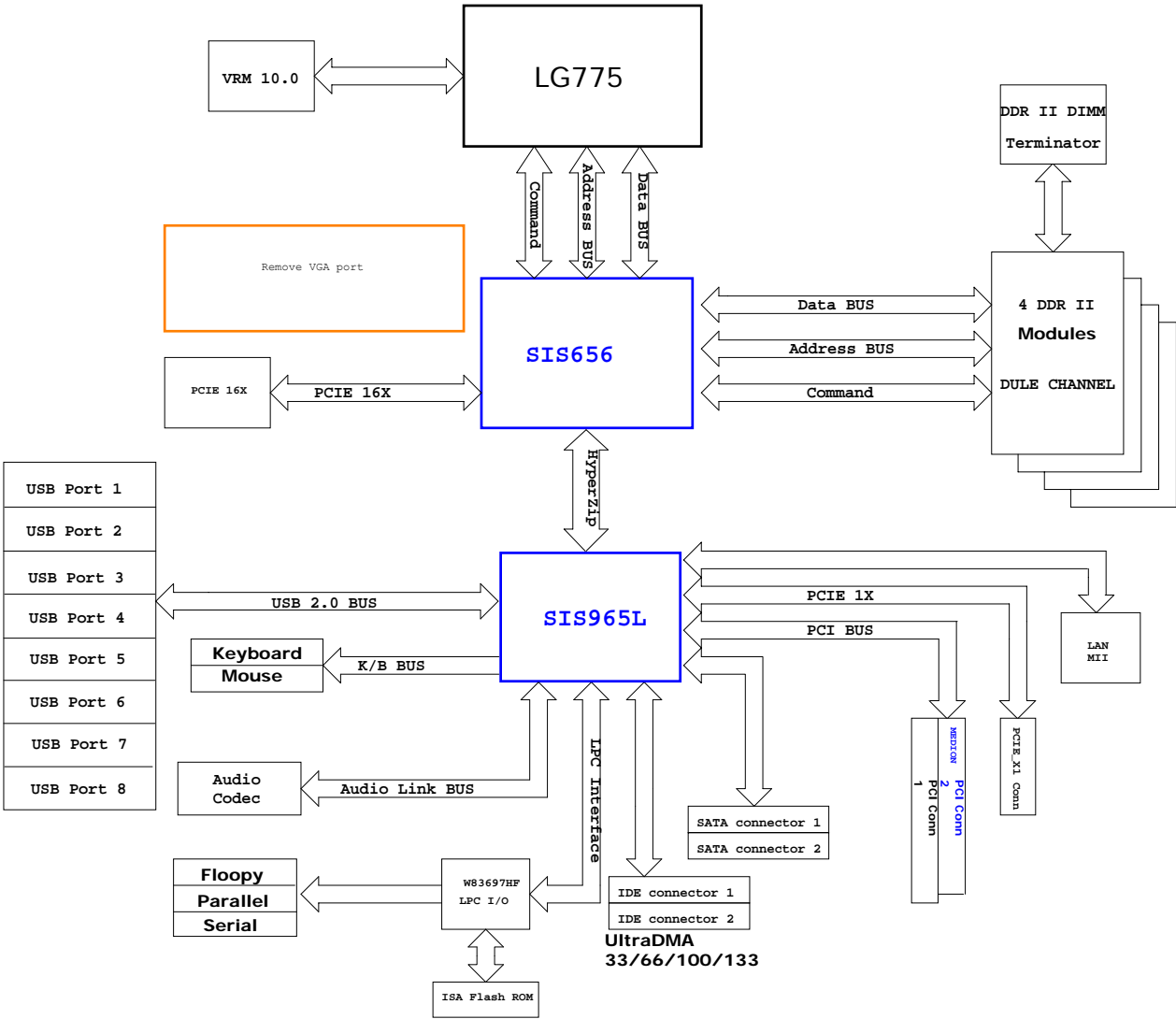
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PCI Routing

PCI 2	INTX# IDSEL=AD23 MASTER=REQ#1 PGNT#1 PCICLK4	INTB# IDSEL=AD21 MASTER=REQ#3 PGNT#3 PCICLK3
PCI 3	INTD# IDSEL=AD19 MASTER=REQ#2 PGNT#2 PCICLK2	INTA# IDSEL=AD20 MASTER=REQ#5 PGNT#5 PCICLK0
1394	INTX# IDSEL=AD22 MASTER=REQ#4 PGNT#4 1394PCLK	 File

Block Diagram

MS-7233 Ver:1.0

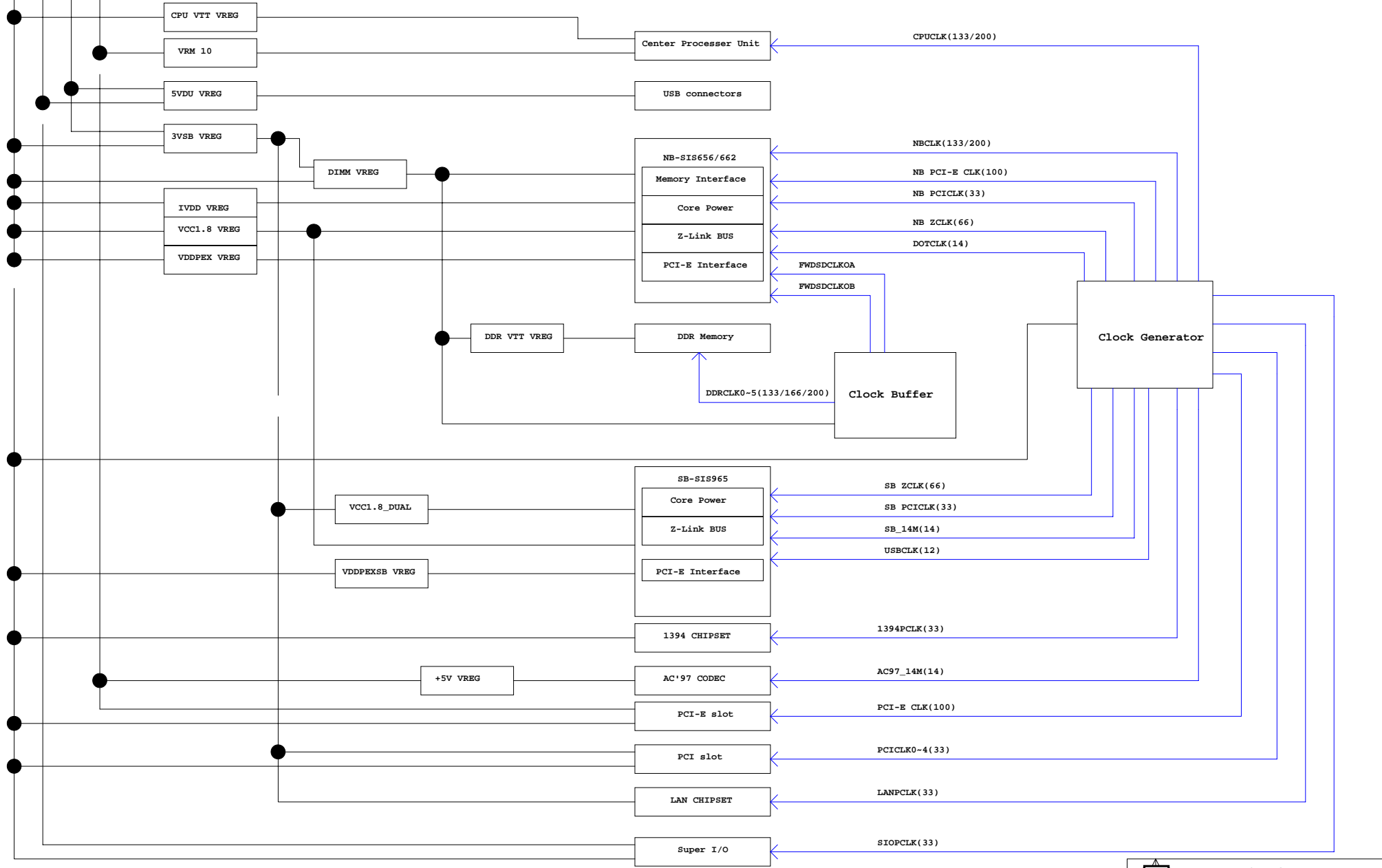


Power Delivery Map

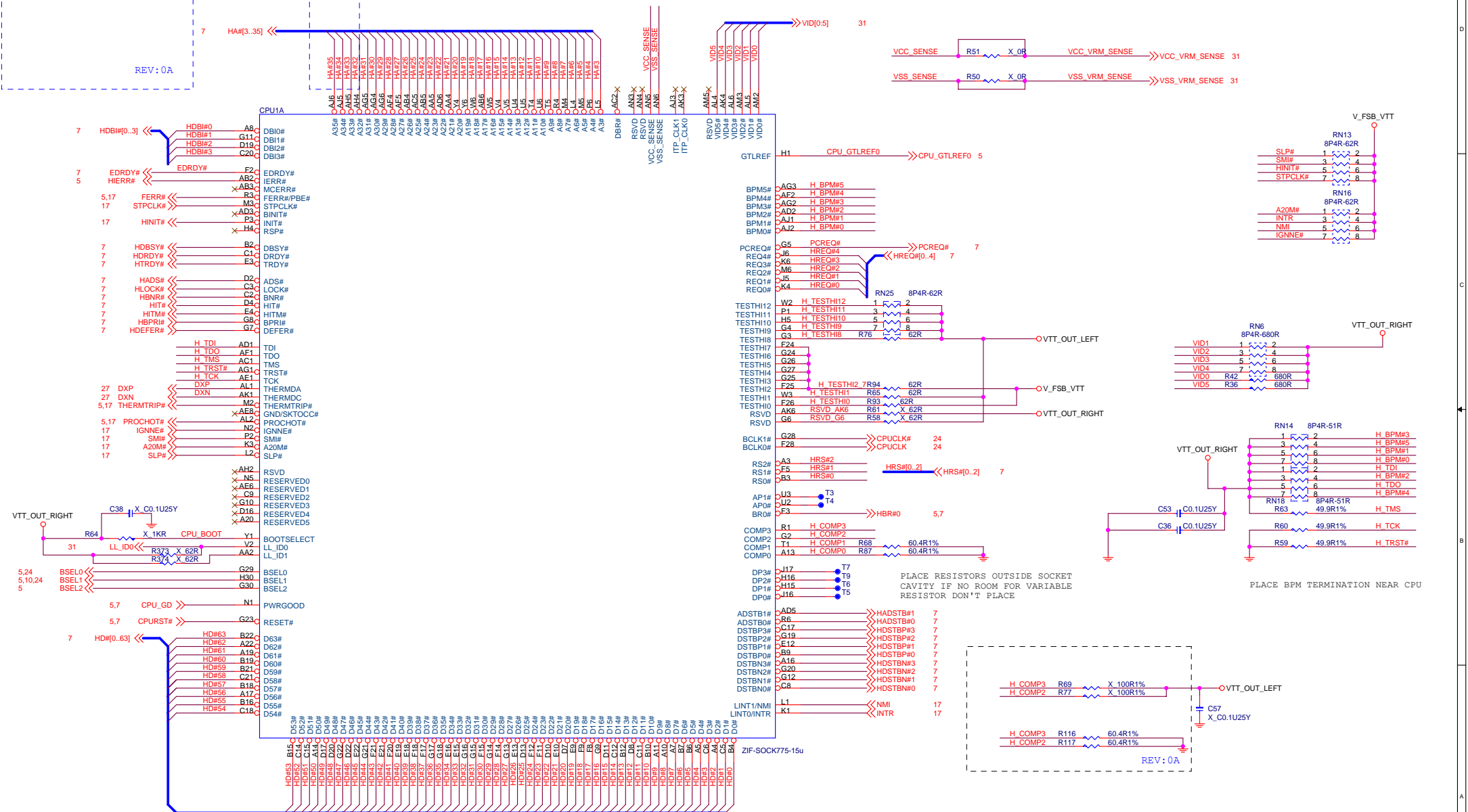
CLOCK Delivery Map

ATX 12V POWER Supply

3.3V	5V	5VSB 1A	12V
------	----	------------	-----

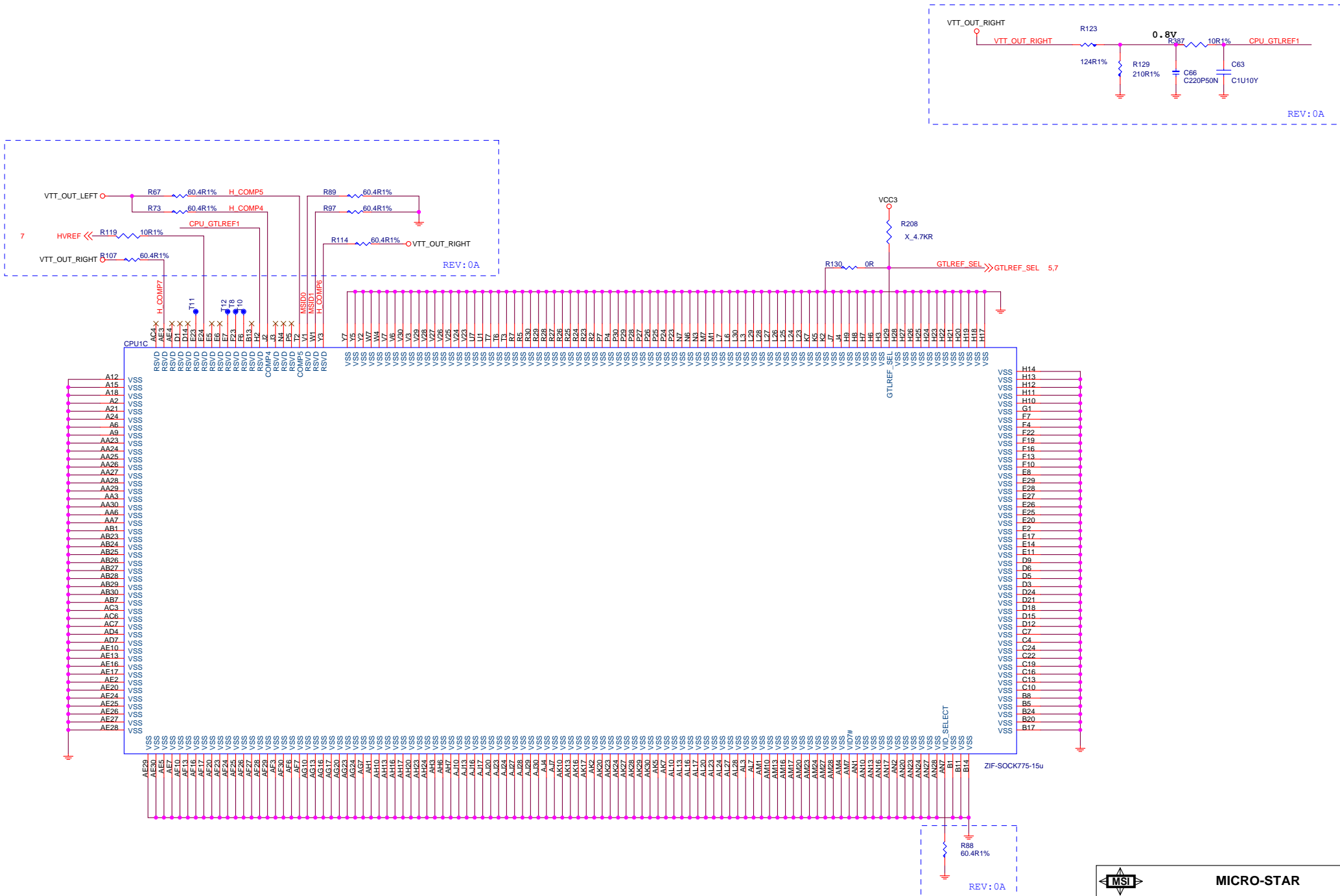


CPU SIGNAL BLOCK



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Title					Intel LGA775 CPU - Signals					
Size		Document Number						Rev		
		MS-7233						1B		
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PCI Express

Host



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656-1 (Host/PCI_Express)

MS-7233

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PCI Express

Host

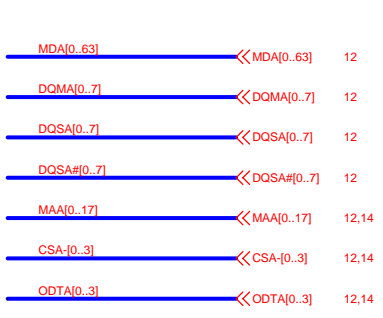


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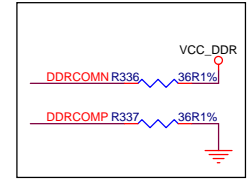
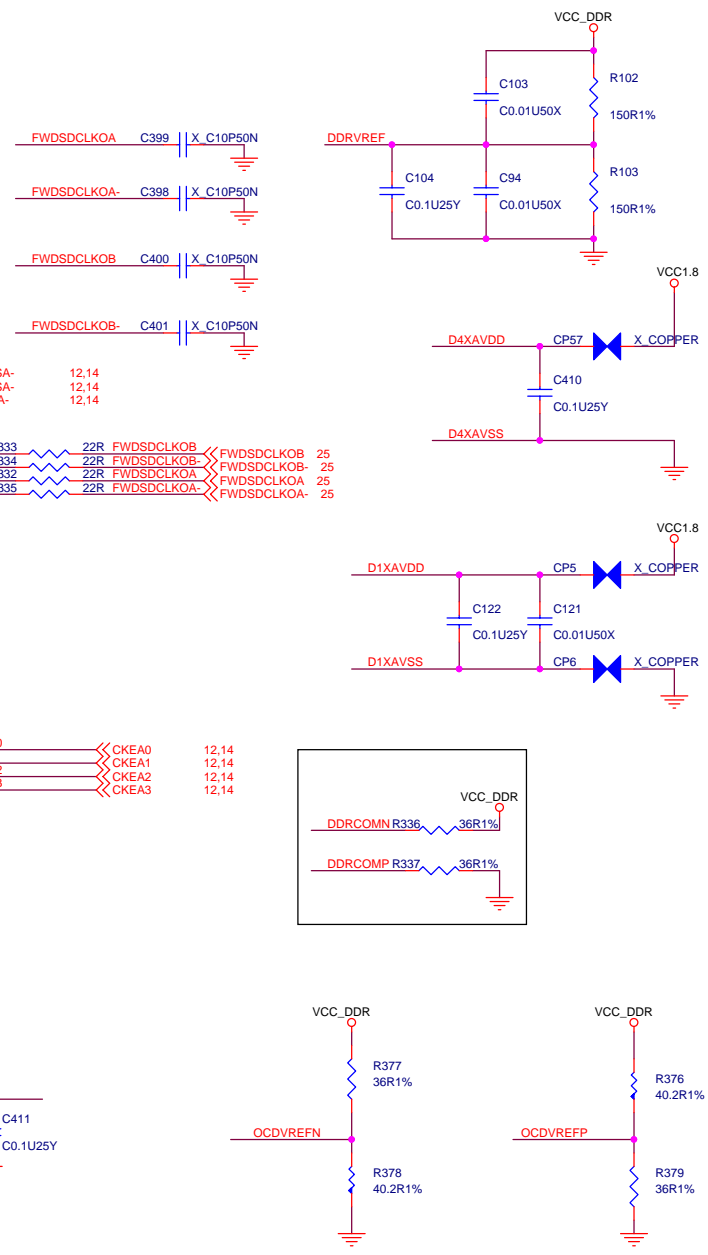
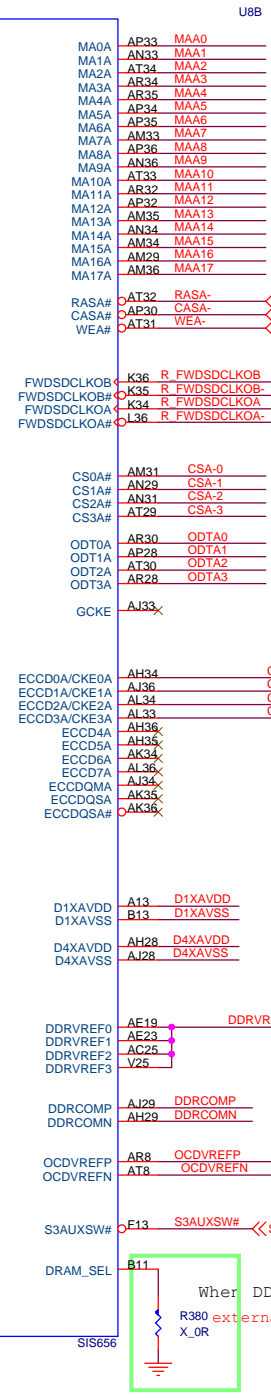
656-1 (Host/PCI_Express)

MS-7233

Title	656-1 (Host/PCI_Express)	Rev	1B
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MDA0	M34	MD0A
MDA1	N36	MD1A
MDA2	R36	MD2A
MDA3	R33	MD3A
MDA4	M36	MD4A
MDA5	M35	MD5A
MDA6	P34	MD6A
MDA7	P34	MD7A
DQMA0	N33	DQM0A
DQSA0	P36	DQS0A
DQSA#0	N32	DQS0A#
MDA8	T39	MD8A
MDA9	T34	MD9A
MDA10	V34	MD10A
MDA11	W36	MD11A
MDA12	R32	MD12A
MDA13	T36	MD13A
MDA14	V36	MD14A
MDA15	V36	MD15A
DQMA1	U36	DQM1A
DQSA1	U32	DQS1A
DQSA#1	U33	DQS1A#
MDA16	Y36	MD16A
MDA17	Y36	MD17A
MDA18	AB35	MD18A
MDA19	AB34	MD19A
MDA20	W33	MD20A
MDA21	W32	MD21A
MDA22	AA32	MD22A
MDA23	AB36	MD23A
DQMA2	V34	DQM2A
DQSA2	AA33	DQS2A
DQSA#2	AA36	DQS2A#
MDA24	AH30	MD24A
MDA25	AJ32	MD25A
MDA26	AM30	MD26A
MDA27	AM30	MD27A
MDA28	AC39	MD28A
MDA29	AH32	MD29A
MDA30	AM32	MD30A
MDA31	AN32	MD31A
DQMA3	AJ30	DQM3A
DQSA3	AL32	DQS3A
DQSA#3	AK32	DQS3A#
MDA32	AH24	MD32A
MDA33	AH23	MD33A
MDA34	AH21	MD34A
MDA35	AM20	MD35A
MDA36	AJ24	MD36A
MDA37	AJ23	MD37A
MDA38	AJ21	MD38A
MDA39	AH22	MD39A
DQMA4	AM22	DQM4A
DQSA4	AJ22	DQS4A
DQSA#4	AK22	DQS4A#
MDA40	AM19	MD40A
MDA41	AT18	MD41A
MDA42	AT16	MD42A
MDA43	AR16	MD43A
MDA44	AT19	MD44A
MDA45	AM19	MD45A
MDA46	AM17	MD46A
MDA47	AM17	MD47A
DQMA5	AR18	DQM5A
DQSA5	AT17	DQS5A
DQSA#5	AP18	DQS5A#
MDA48	AN15	MD48A
MDA49	AM15	MD49A
MDA50	AM13	MD50A
MDA51	AT12	MD51A
MDA52	AP16	MD52A
MDA53	AT15	MD53A
MDA54	AN13	MD54A
MDA55	AT13	MD55A
DQMA6	AT14	DQM6A
DQSA6	AP14	DQS6A
DQSA#6	AR14	DQS6A#
MDA56	AT11	MD56A
MDA57	AT11	MD57A
MDA58	AR9	MD58A
MDA59	AP9	MD59A
MDA60	AR12	MD60A
MDA61	AP12	MD61A
MDA62	AP10	MD62A
MDA63	AT9	MD63A
DQMA7	AM11	DQM7A
DQSA7	AR10	DQS7A
DQSA#7	AT10	DQS7A#



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Title656-2 (SDRAM A)

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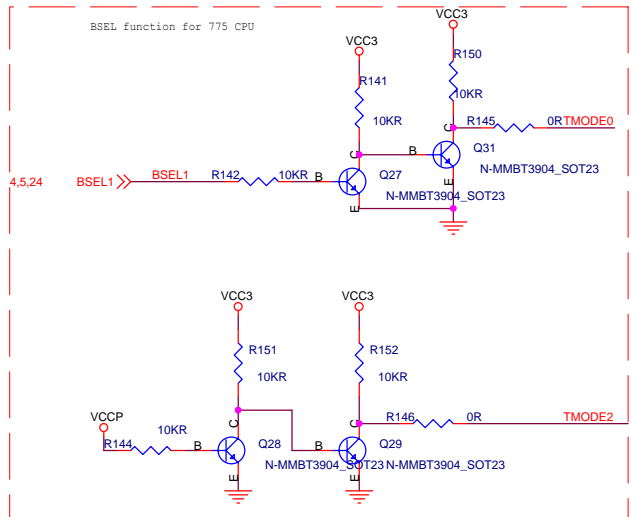
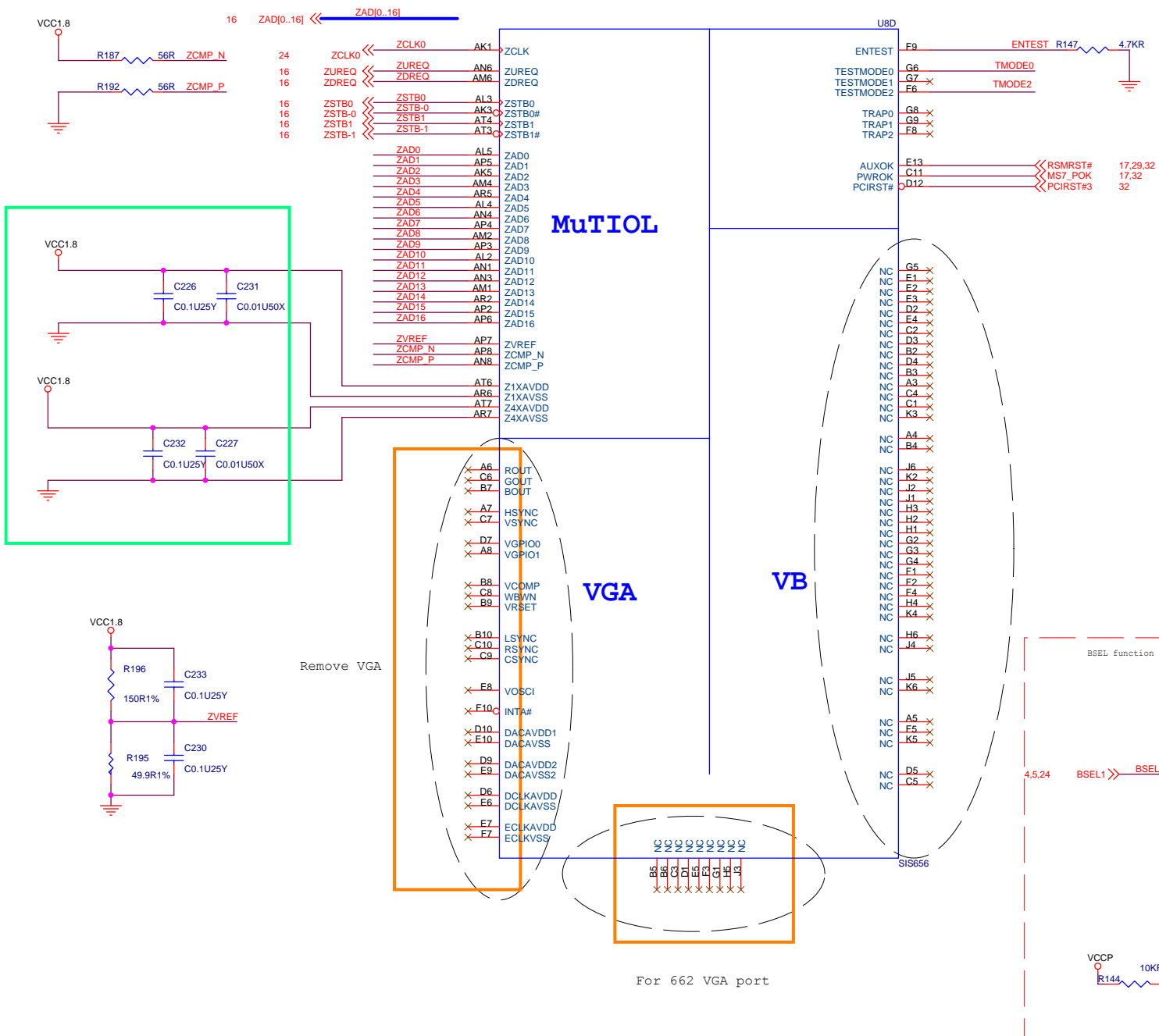
MDB[0..63] << MDB[0..63] 13
DQMB[0..7] << DQMB[0..7] 13
DQSB[0..7] << DQSB[0..7] 13
DQSB#[0..7] << DQSB#[0..7] 13
MAB[0..17] << MAB[0..17] 13,15
CSB-[0..3] << CSB-[0..3] 13,15
ODTB[0..3] << ODTB[0..3] 13,15

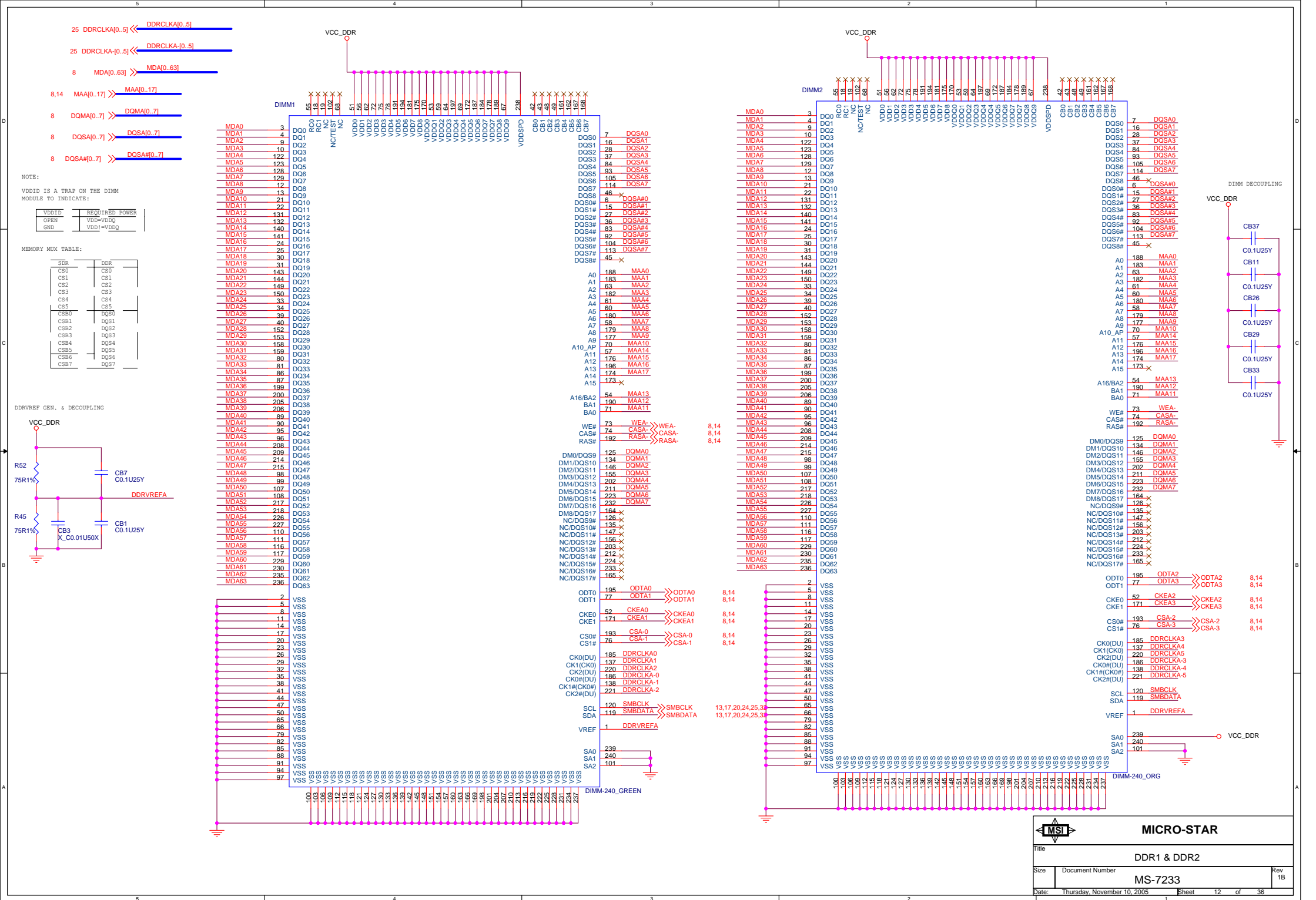
MDB0 N29 MD0B
MDB1 M28 MD1B
MDB2 P28 MD2B
MDB3 R28 MD3B
MDB4 M30 MD4B
MDB5 M29 MD5B
MDB6 P29 MD6B
MDB7 R29 MD7B
DQMB0 N28 DQM0B
DQSB0 P30 DQS0B
DQSB#0 P32 DQS0B#
MDB8 T29 MD8B
MDB9 U29 MD9B
MDB10 W29 MD10B
MDB11 V28 MD11B
MDB12 T32 MD12B
MDB13 V30 MD13B
MDB14 V30 MD14B
MDB15 V29 MD15B
DQMB1 T28 DQM1B
DQSB1 V32 DQS1B
DQSB#1 U28 DQS1B#
MDB16 Y30 MD16B
MDB17 Y29 MD17B
MDB18 AB29 MD18B
MDB19 AC29 MD19B
MDB20 W28 MD20B
MDB21 Y32 MD21B
MDB22 AB32 MD22B
MDB23 AB30 MD23B
DQMB2 AA29 DQM2B
DQSB2 AA28 DQS2B
DQSB#2 Y28 DQS2B#
MDB24 AD32 MD24B
MDB25 AD30 MD25B
MDB26 AE30 MD26B
MDB27 AF29 MD27B
MDB28 AB28 MD28B
MDB29 AC28 MD29B
MDB30 AE28 MD30B
MDB31 AF32 MD31B
DQMB3 AD29 DQM3B
DQSB3 AD28 DQS3B
DQSB#3 AE29 DQS3B#
MDB32 AJ27 MD32B
MDB33 AM26 MD33B
MDB34 AM24 MD34B
MDB35 AK24 MD35B
MDB36 AM28 MD36B
MDB37 AK28 MD37B
MDB38 AH26 MD38B
MDB39 AH25 MD39B
DQMB4 AK26 DQM4B
DQSB4 AJ25 DQS4B
DQSB#4 AJ26 DQS4B#
MDB40 AJ19 MD40B
MDB41 AH20 MD41B
MDB42 AH18 MD42B
MDB43 AH17 MD43B
MDB44 AK20 MD44B
MDB45 AJ20 MD45B
MDB46 AJ18 MD46B
MDB47 AJ17 MD47B
DQMB5 AH19 DQM5B
DQSB5 AK18 DQS5B
DQSB#5 AM18 DQS5B#
MDB48 AJ16 MD48B
MDB49 AJ15 MD49B
MDB50 AJ13 MD50B
MDB51 AH14 MD51B
MDB52 AM16 MD52B
MDB53 AK16 MD53B
MDB54 AK14 MD54B
MDB55 AJ14 MD55B
DQMB6 AH16 DQM6B
DQSB6 AM14 DQS6B
DQSB#6 AH15 DQS6B#
MDB56 AK12 MD56B
MDB57 AJ12 MD57B
MDB58 AN9 MD58B
MDB59 AM9 MD59B
MDB60 AH13 MD60B
MDB61 AM12 MD61B
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DQSB#7 AH12 DQS7B#

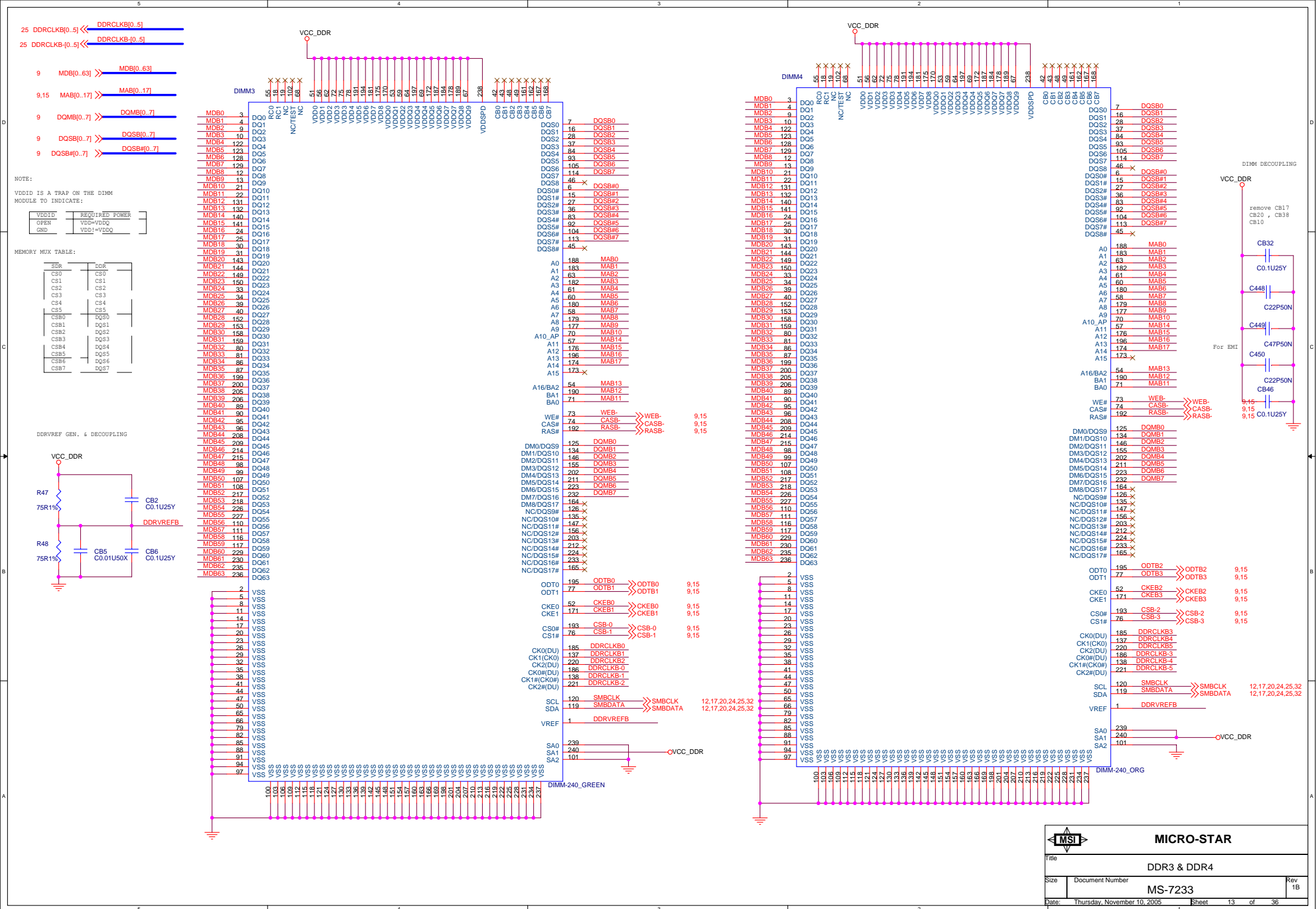
U8C
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MA1B AN25 MAB1
MA2B AM25 MAB2
MA3B AT26 MAB3
MA4B AR26 MAB4
MA5B AP26 MAB5
MA6B AT27 MAB6
MA7B AM27 MAB7
MA8B AN27 MAB8
MA9B AG32 MAB9
MA10B AP24 MAB10
MA11B AT24 MAB11
MA12B AR24 MAB12
MA13B AG36 MAB13
MA14B AT28 MAB14
MA15B AG33 MAB15
MA16B AN21 MAB16
MA17B AF34 MAB17
RASB# AT23 RASB- << RASB- 13,15
CASB# AR22 CASB- << CASB- 13,15
WEB# AT22 WEB- << WEB- 13,15
ECCD0B/CKE0B AC32 CKEB0 << CKEB0 13,15
ECCD1B/CKE1B AD36 CKEB1 << CKEB1 13,15
ECCD2B/CKE2B AF36 CKEB2 << CKEB2 13,15
ECCD3B/CKE3B AF35 CKEB3 << CKEB3 13,15
ECCD4B AC36
ECCD5B AC33
ECCD6B AE33
ECCD7B AE32
ECCD0MB AD35
ECCDQSB AE36
ECCDQSB# AD34
CS0B# AN23 CSB-0
CS1B# AM21 CSB-1
CS2B# AM23 CSB-2
CS3B# AT20 CSB-3
ODT0B AP22 ODTB0
ODT1B AR20 ODTB1
ODT2B AT21 ODTB2
ODT3B AP20 ODTB3



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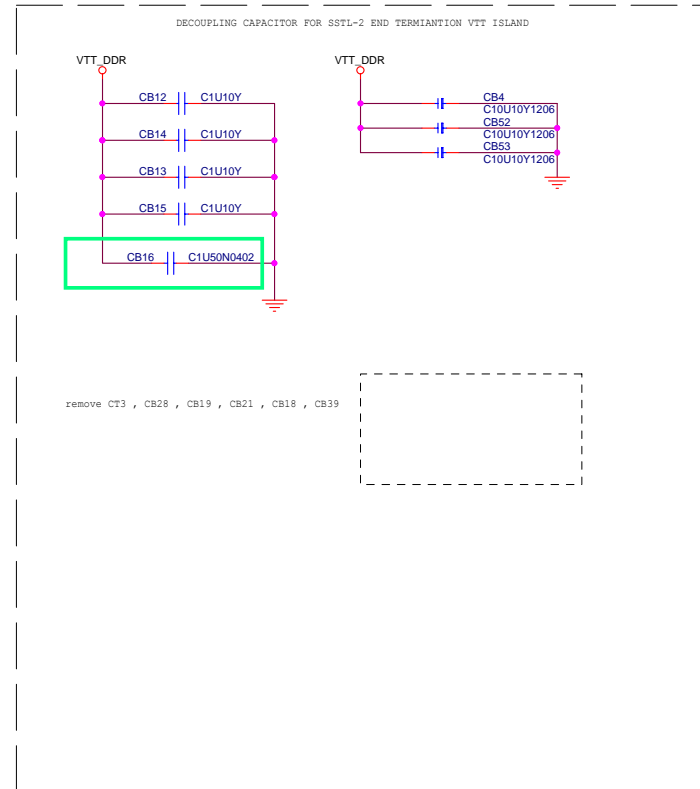
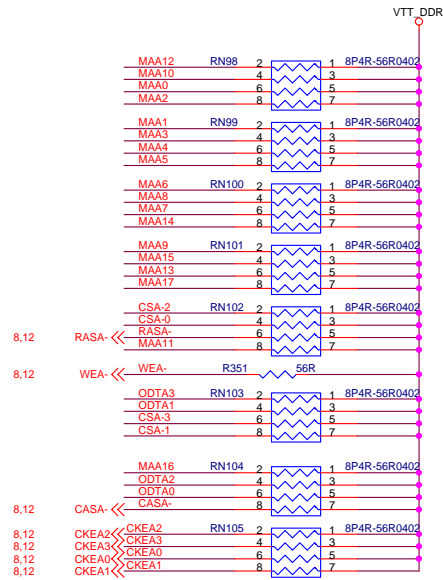


DDR TERMINATOR

SSTL-2 Termination Resistors

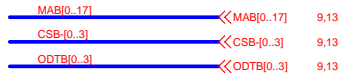


	SDR			DDR			
MD/DQM (/DQS)	LV-CMOS		0/10/-	SSTL-2		0	03
MA/Control	LV-CMOS		0	SSTL-2		0	03
CS	LV-CMOS		0	SSTL-2		0	47
VME	0D 3.3V			0D 2.5V			

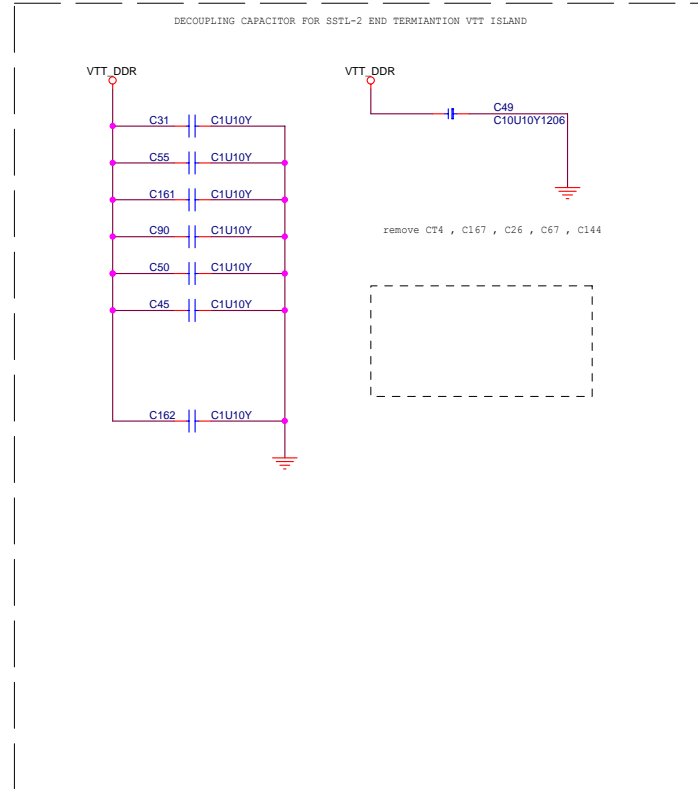
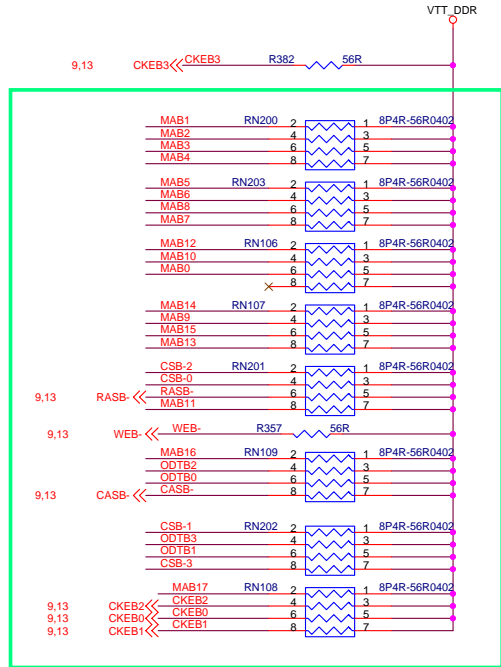


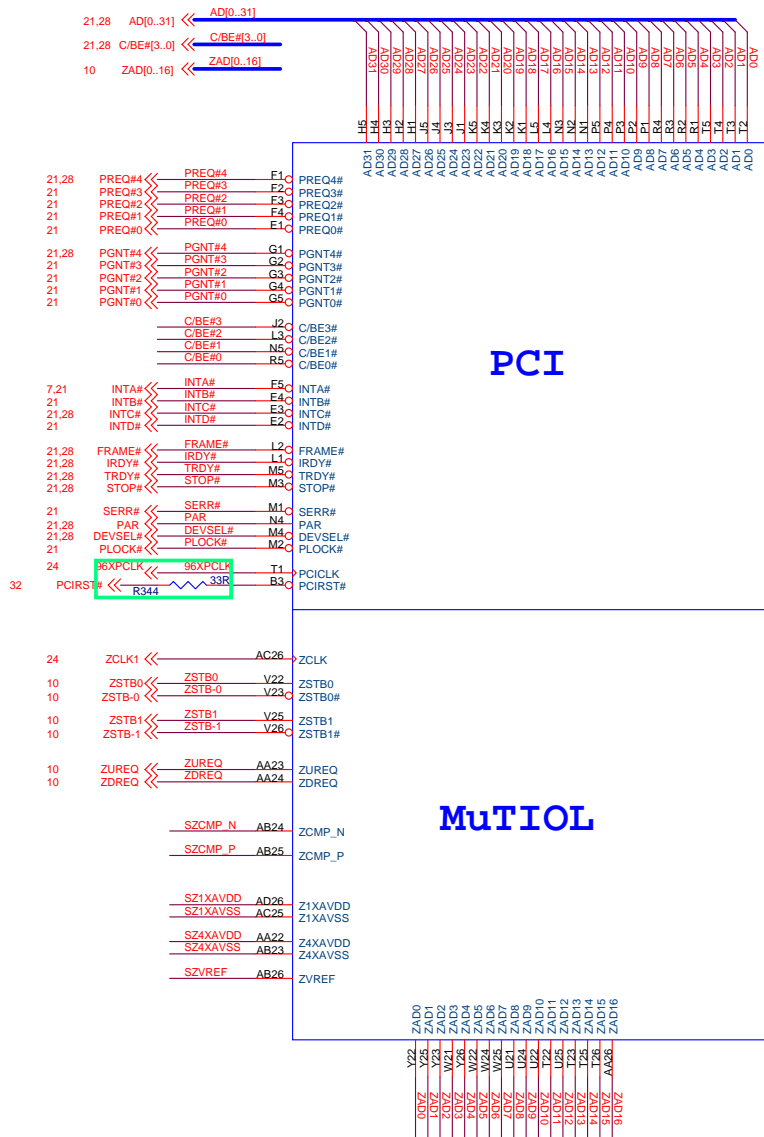
DDR TERMINATOR

SSTL-2 Termination Resistors

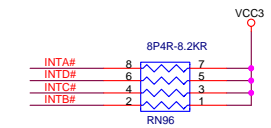
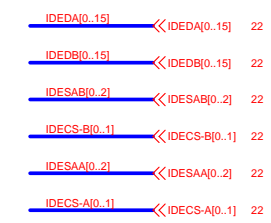
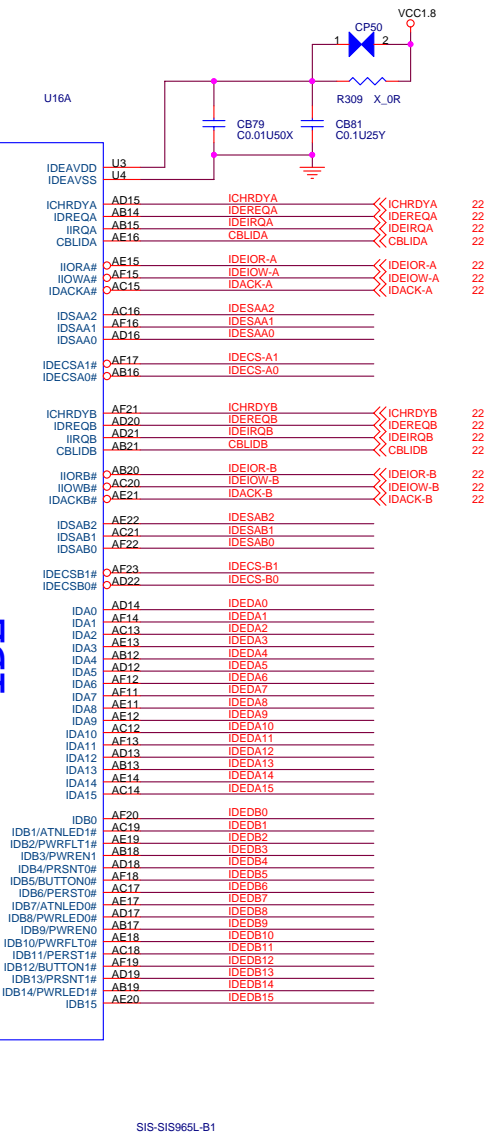


	DDR		DDR		
AD/DQM (/DQS)	LV-CMOS	R _s	SSTL-2	R _s	R _{tt}
BA/Control	LV-CMOS	0/10/-	SSTL-2	10	33
CS	LV-CMOS	10	SSTL-2	10	33
CKE	1D 3.3V	0	SSTL-2	1D 2.5V	47

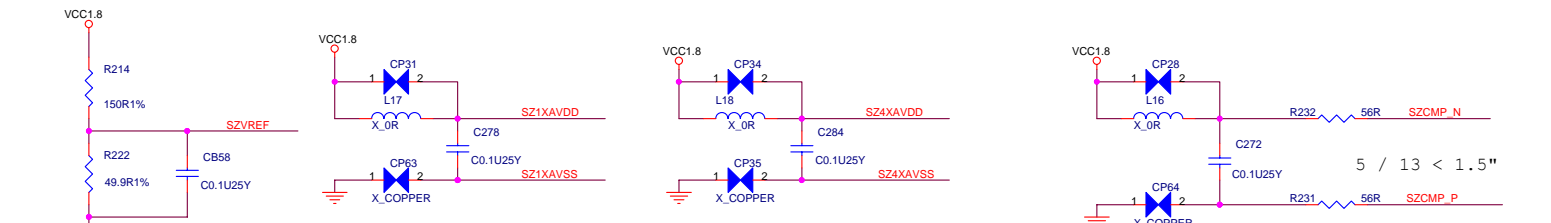




IDE



Put near SB SiS 965 Chip.
delete STB0/-0/1/-1 pull-up circuit



Analog Power supplies of Transzip function for 964 Chip.

12 / 15 < 1.5"

4 HINIT# AC23
4 A20M# AE26
4 SMI# AD23
4 INTR AC22
4 NMI AE25
4.5 IGNNE# AF25
4.5 FERR# AE24
4 STPCLK# AD24
4 SLP# AD24

VCC3 R220 10KR AF24
4.5 PROCHOT# AD25
4.5 THERMTRIP# AC24

27 LAD0 Y5
27 LAD1 Y4
27 LAD2 AA2
27 LAD3 AA3
27 LFRAME# AA1
27 LDRQ# AA4
27 LDRQ# SIRO# AA5

OSC32KHI C1
OSC32KHO C2
BATOK D4
ALL PWGRD D2
RTCVDV C3
RTCVDSS D3
SMBDATA W5
SMBCLK W4
AC_SDIN0 E6
AC_SDIN1 B4
AC_SDOUT W3
AC_SYNC W2
AC_RST# B5
AC_BITCLK W1
SB14M Y2
SPK D1
SPK Y1
PWRBTN# D5
PME# A6
PSON# E7
RSMRST# X
C327 X_C0.01U50X
GPIO13 B2
GPIO14 A5
KB DAT C7
KB CLK B7
MS DAT D7
MS CLK D6

AC_SDIN0 E6
AC_SDIN1 B4
AC_SDOUT W3
AC_SYNC W2
AC_RST# B5
AC_BITCLK W1
SB14M Y2
SPK D1
SPK Y1
PWRBTN# D5
PME# A6
PSON# E7
RSMRST# X
C327 X_C0.01U50X
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GPIO14 A5
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KB CLK B7
MS DAT D7
MS CLK D6

AC_RST# B5
AC_BITCLK W1
SB14M Y2
SPK D1
SPK Y1
PWRBTN# D5
PME# A6
PSON# E7
RSMRST# X
C327 X_C0.01U50X
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GPIO14 A5
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KB CLK B7
MS DAT D7
MS CLK D6

AC_RST# B5
AC_BITCLK W1
SB14M Y2
SPK D1
SPK Y1
PWRBTN# D5
PME# A6
PSON# E7
RSMRST# X
C327 X_C0.01U50X
GPIO13 B2
GPIO14 A5
KB DAT C7
KB CLK B7
MS DAT D7
MS CLK D6

AC_RST# B5
AC_BITCLK W1
SB14M Y2
SPK D1
SPK Y1
PWRBTN# D5
PME# A6
PSON# E7
RSMRST# X
C327 X_C0.01U50X
GPIO13 B2
GPIO14 A5
KB DAT C7
KB CLK B7
MS DAT D7
MS CLK D6

AC_RST# B5
AC_BITCLK W1
SB14M Y2
SPK D1
SPK Y1
PWRBTN# D5
PME# A6
PSON# E7
RSMRST# X
C327 X_C0.01U50X
GPIO13 B2
GPIO14 A5
KB DAT C7
KB CLK B7
MS DAT D7
MS CLK D6

AC_RST# B5
AC_BITCLK W1
SB14M Y2
SPK D1
SPK Y1
PWRBTN# D5
PME# A6
PSON# E7
RSMRST# X
C327 X_C0.01U50X
GPIO13 B2
GPIO14 A5
KB DAT C7
KB CLK B7
MS DAT D7
MS CLK D6

AC_RST# B5
AC_BITCLK W1
SB14M Y2
SPK D1
SPK Y1
PWRBTN# D5
PME# A6
PSON# E7
RSMRST# X
C327 X_C0.01U50X
GPIO13 B2
GPIO14 A5
KB DAT C7
KB CLK B7
MS DAT D7
MS CLK D6

AC_RST# B5
AC_BITCLK W1
SB14M Y2
SPK D1
SPK Y1
PWRBTN# D5
PME# A6
PSON# E7
RSMRST# X
C327 X_C0.01U50X
GPIO13 B2
GPIO14 A5
KB DAT C7
KB CLK B7
MS DAT D7
MS CLK D6

CPU_S

APIC

LPC

RTC

SMBUS

AC'97

ACPI/Others

KBC

Keyboard

/Mouse

GPIO

GMII/RGMII

PCI

Express

GPIO

U16B

TXCLK B8
GTCLK A10
EXTCLK A13

TXEN B10
TXER D11

TXD0 A8
TXD1 C9
TXD2 A9
TXD3 E9
TXD4 D8
TXD5 E10
TXD6 D10
TXD7 C10

RGMCMCP N
RGMCMCP P
RGMVREF

RXCCLK A11
RXD0 C13
RXD1 C12
RXD2 A12
RXD3 B12
RXD4 D13
RXD5 E14
RXD6 E13
RXD7 E12

COL F11
CRS F12
MDC F13
MDIO F14

PRX0+ M26
PRX0- M25
PTX0+ N24
PTX0- N23
PRX1+ K26
PRX1- K25
PTX1+ L24
PTX1- L23

NC11 F26
NC10 F25
NC9 G24
NC8 G23
NC7 H26
NC6 H25
NC5 J24
NC4 J23

PCLK100P P26
PCLK100N P25
PEXTRXAVDD P25
PEXTRXAVSS P25
RSET0 P22
RSET1 P21

PECLK2 P26
PECLK2 P25
PERSET0 P22
PERSET1 P21

GPIO0/SPDIF U5
GPIO1/LDRQ1# AA6
GPIO2/THERM# V5
GPIO3/EXTSMI# V4
GPIO4/CLKRUN# V3
GPIO5/PREQ5# V2
GPIO6/PGNT5# V1
GPIO7 GPIO8
GPIO8/RING C6
GPIO9/AC_SDIN2 C4
GPIO10/AC_SDIN3 E6
GPIO11/OSC25M/STP_PC# F6
GPIO12/CPUSTP# E5

GPIO0/SPDIF U5
GPIO1/LDRQ1# AA6
GPIO2/THERM# V5
GPIO3/EXTSMI# V4
GPIO4/CLKRUN# V3
GPIO5/PREQ5# V2
GPIO6/PGNT5# V1
GPIO7 GPIO8
GPIO8/RING C6
GPIO9/AC_SDIN2 C4
GPIO10/AC_SDIN3 E6
GPIO11/OSC25M/STP_PC# F6
GPIO12/CPUSTP# E5

GPIO0/SPDIF U5
GPIO1/LDRQ1# AA6
GPIO2/THERM# V5
GPIO3/EXTSMI# V4
GPIO4/CLKRUN# V3
GPIO5/PREQ5# V2
GPIO6/PGNT5# V1
GPIO7 GPIO8
GPIO8/RING C6
GPIO9/AC_SDIN2 C4
GPIO10/AC_SDIN3 E6
GPIO11/OSC25M/STP_PC# F6
GPIO12/CPUSTP# E5

GPIO0/SPDIF U5
GPIO1/LDRQ1# AA6
GPIO2/THERM# V5
GPIO3/EXTSMI# V4
GPIO4/CLKRUN# V3
GPIO5/PREQ5# V2
GPIO6/PGNT5# V1
GPIO7 GPIO8
GPIO8/RING C6
GPIO9/AC_SDIN2 C4
GPIO10/AC_SDIN3 E6
GPIO11/OSC25M/STP_PC# F6
GPIO12/CPUSTP# E5

GPIO0/SPDIF U5
GPIO1/LDRQ1# AA6
GPIO2/THERM# V5
GPIO3/EXTSMI# V4
GPIO4/CLKRUN# V3
GPIO5/PREQ5# V2
GPIO6/PGNT5# V1
GPIO7 GPIO8
GPIO8/RING C6
GPIO9/AC_SDIN2 C4
GPIO10/AC_SDIN3 E6
GPIO11/OSC25M/STP_PC# F6
GPIO12/CPUSTP# E5

GPIO0/SPDIF U5
GPIO1/LDRQ1# AA6
GPIO2/THERM# V5
GPIO3/EXTSMI# V4
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GPIO10/AC_SDIN3 E6
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GPIO8/RING C6
GPIO9/AC_SDIN2 C4
GPIO10/AC_SDIN3 E6
GPIO11/OSC25M/STP_PC# F6
GPIO12/CPUSTP# E5

20040319
SiS garychen [garychen@sis.com] suggestion :
I think Pull-up resistors in LADs, LDREQ, and SRQ, are not necessary. However, I still recommend you to have these pads reserved in case of any problems in the future.

GPI5 GPO5	APC1[2] = 0 , APC168[5] = 1
GPI6 GPO6	APC1[2] = 0 , APC168[6] = 1
PREQ5# PGNT#5	APC1[2] = 1

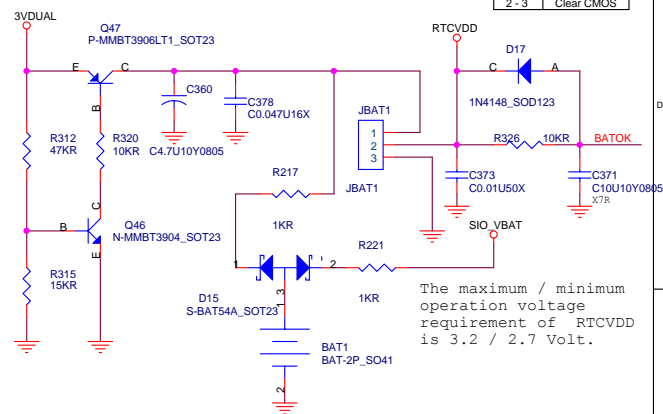
Power on --> APC1[2] = 0h
ACPI68 = Fh

RTCVDV should be more than 30 mils width

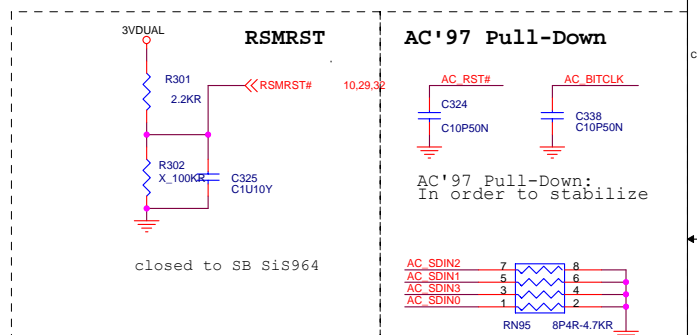
BATTERY BLOCK

CMOS CLEAR JUMPER

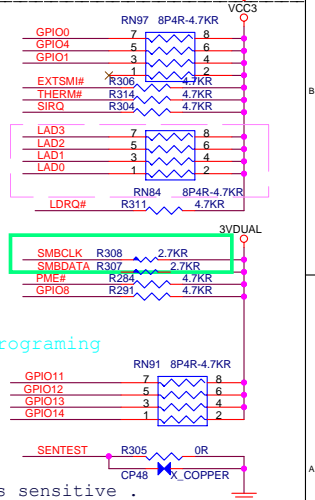
JBAT1	Clear CMOS
1-2	Normal
2-3	Clear CMOS



The maximum / minimum operation voltage requirement of RTCVDV is 3.2 / 2.7 Volt.

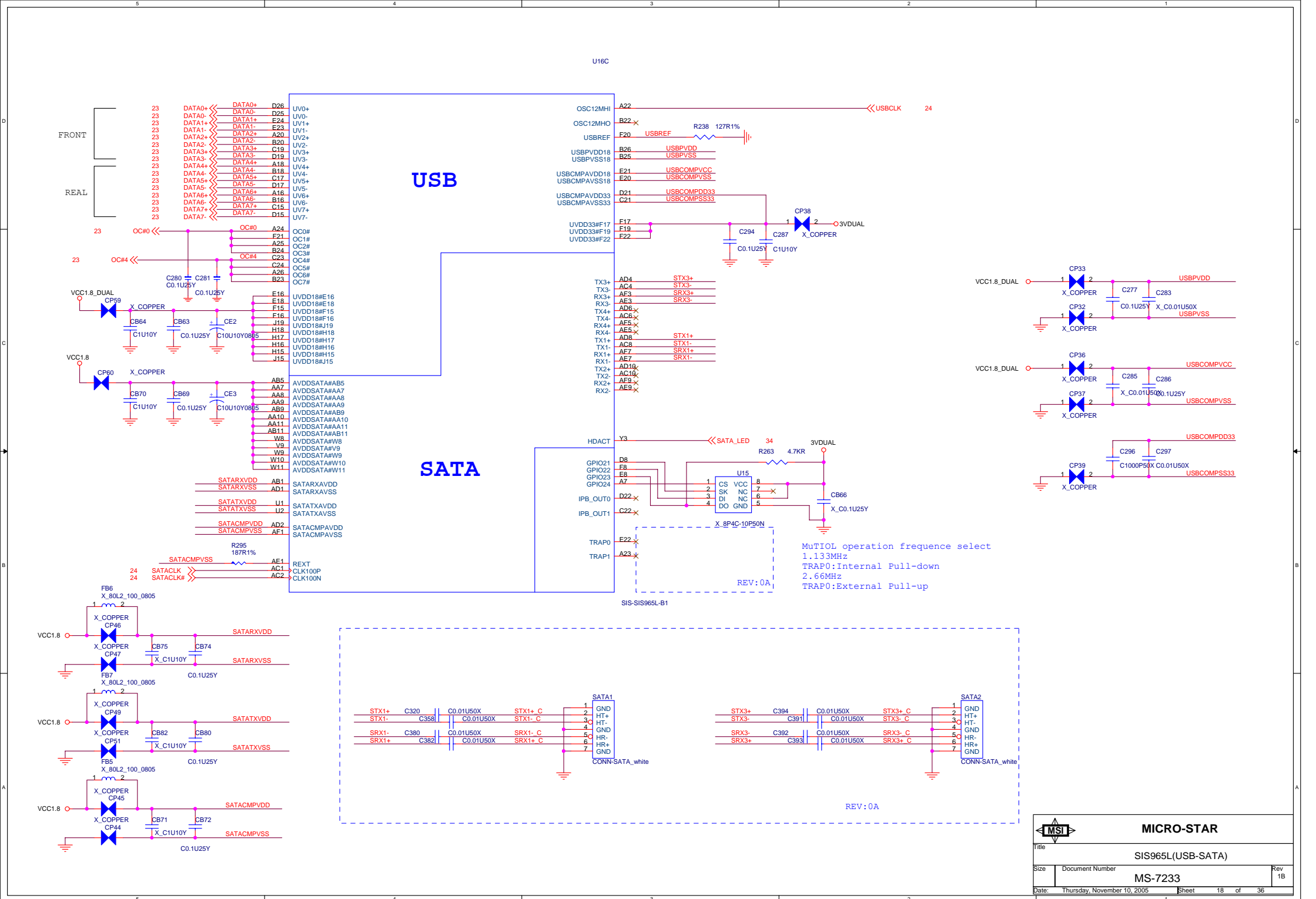


NEED NOT to place close to SB Sis964
GPIO 0~7 INTERNAL PULL UP
GPIO 9,10 INTERNAL PULL DOWN
Register 72 ~ 73



ENTEST pin is sensitive .
5 / 15

MSI MICRO-STAR		
Title: SIS965L(MISC.)		
Size	Document Number	Rev
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Date:	Thursday, November 10, 2005	Sheet 17 of 36

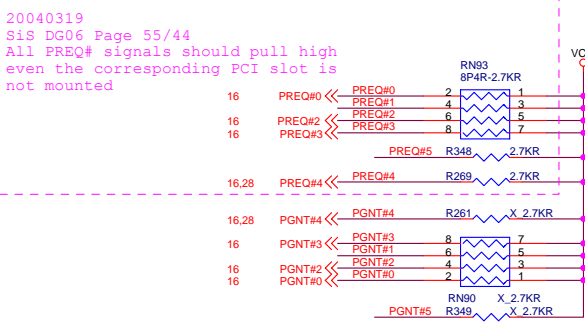
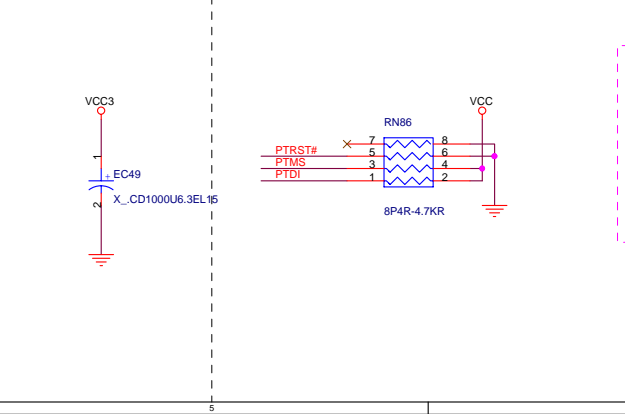
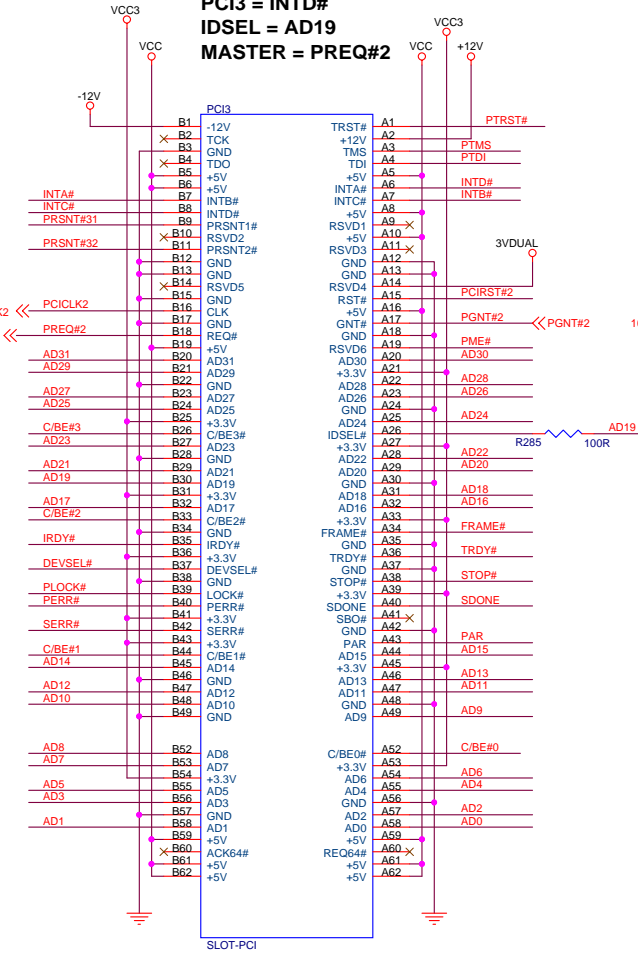
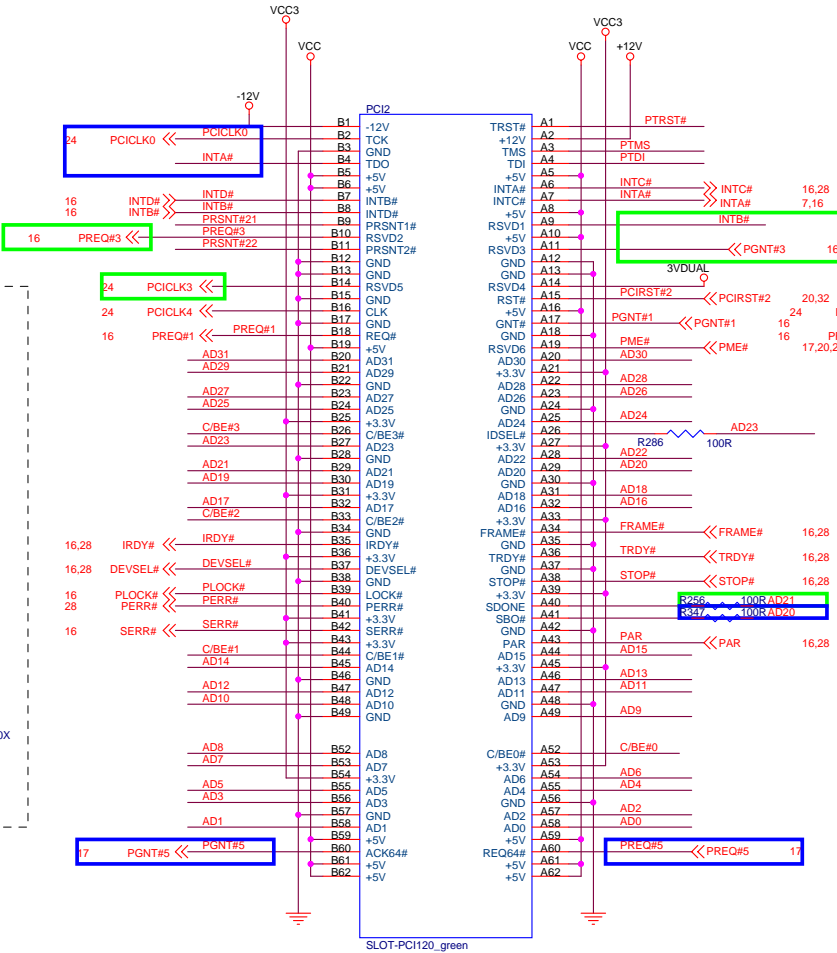
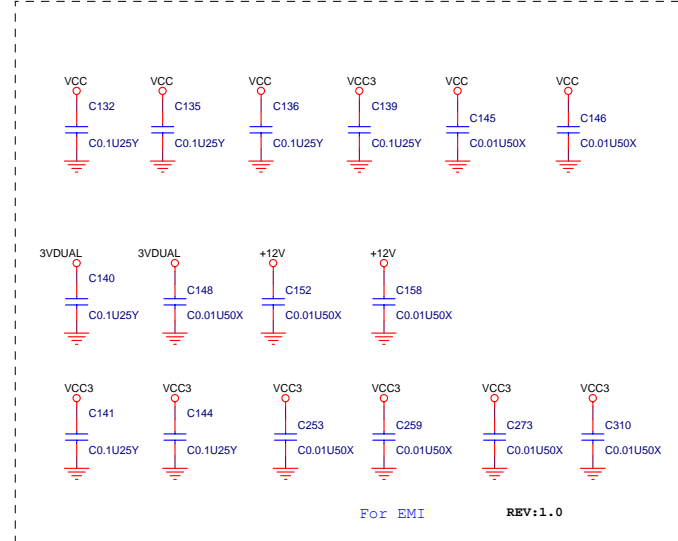


PCI SLOT 2,3(PCI VER:2.3 COMPLY)

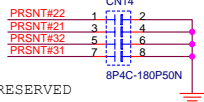
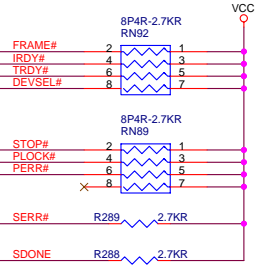
PCI2 = INTCA# and INTB#
IDSEL = AD23 and AD21
MASTER = PREQ#1 and PREQ#3

16,28 AD[0..31] << AD[0..31]
16,28 C/BE#[3..0] << C/BE#[3..0]

PCI3 = INTD#
IDSEL = AD19
MASTER = PREQ#2



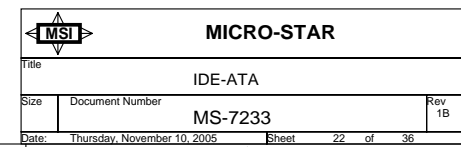
PCI BUS PULL-UP



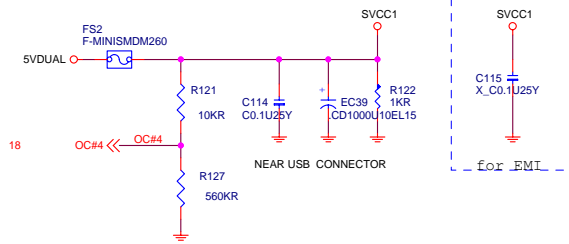
MICRO-STAR

Title			PCI slot 1 & 2 & 3		
Size			MS-7233		
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Rev			18		

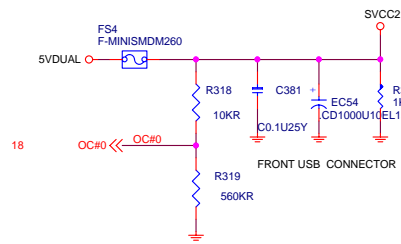
20040319
SiS AP note : A964008



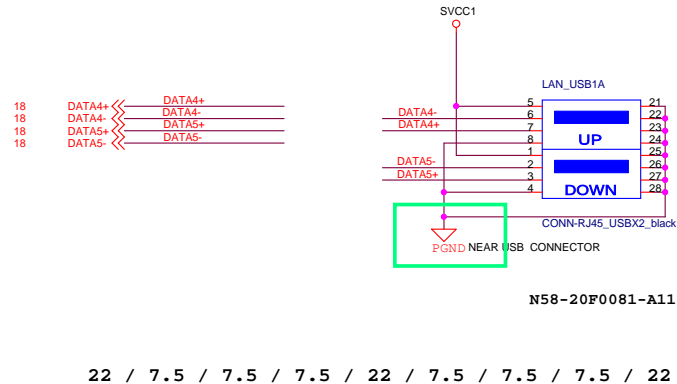
POWER CIRCUIT FOR USB PORT 4,5,6,7



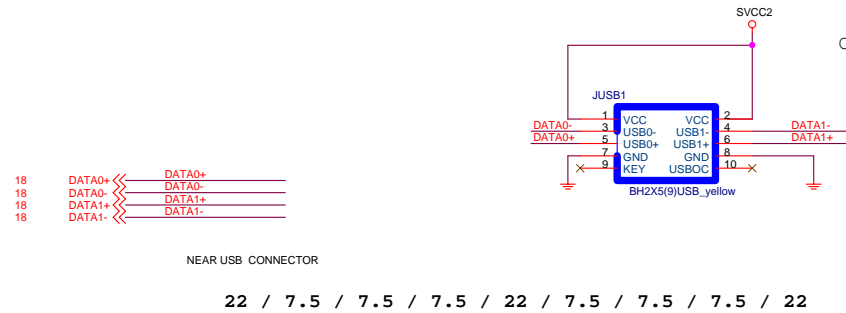
POWER CIRCUIT FOR USB PORT 0,1,2,3



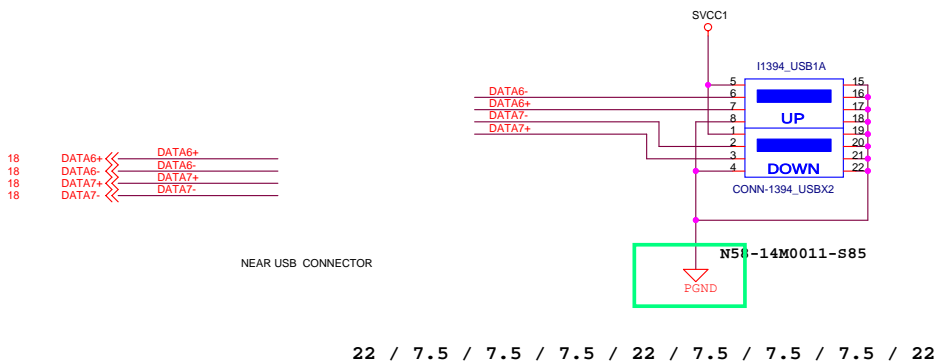
REAR PANEL USB CONNECTOR FOR USB PORT 4,5



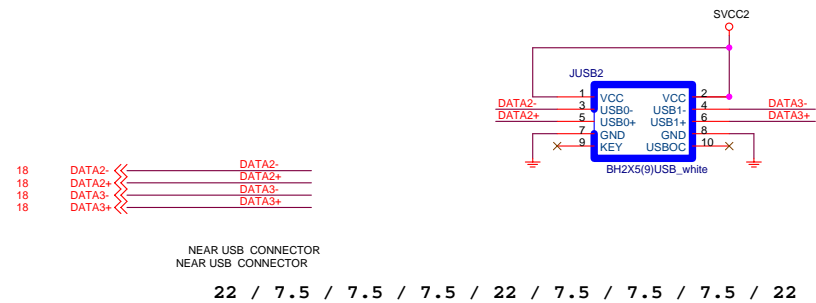
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



REAR PANEL USB CONNECTOR FOR USB PORT 6,7

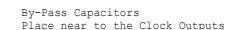


FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



OPTIONS

1. ICS953401

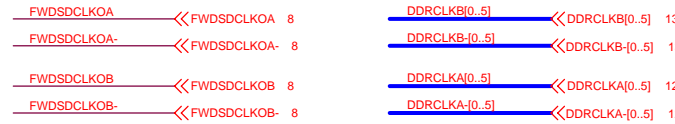
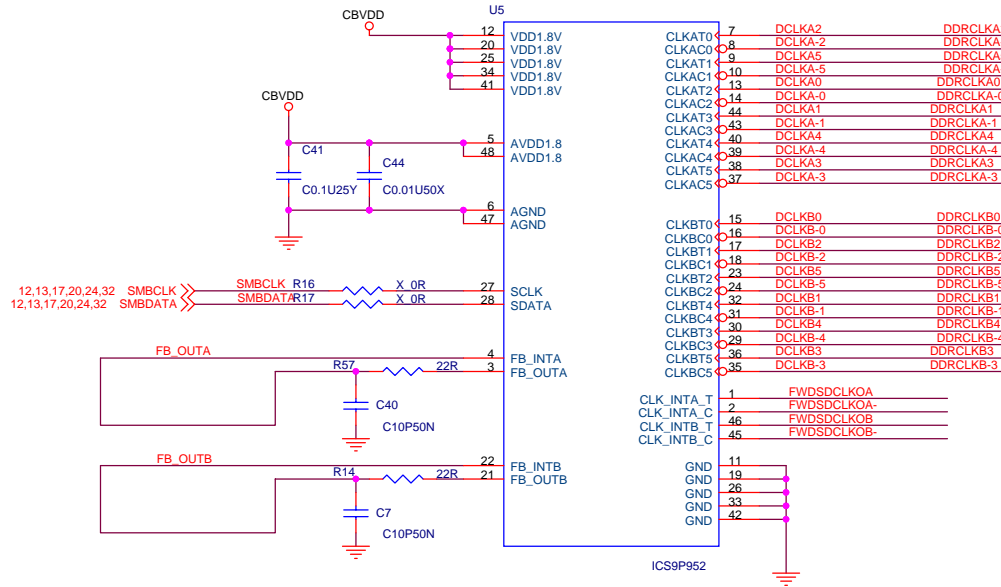
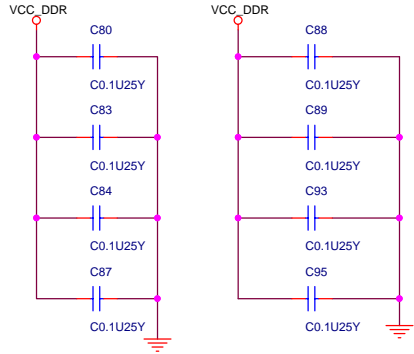


PCICLK0	PCI2 master3
PCICLK2	PCI3
PCICLK3	PCI2 master2
PCICLK4	PCI2 master1

Clock Buffer (DDR II)

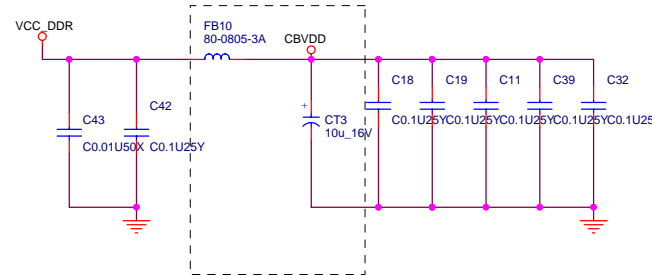
By-Pass Capacitors
Place near to the Clock Buffer

Remove damping resistor



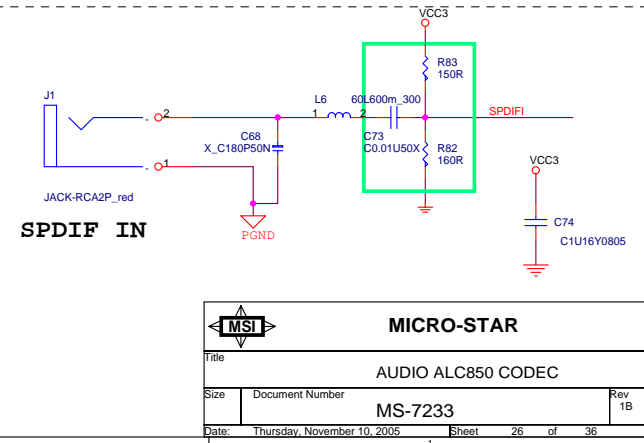
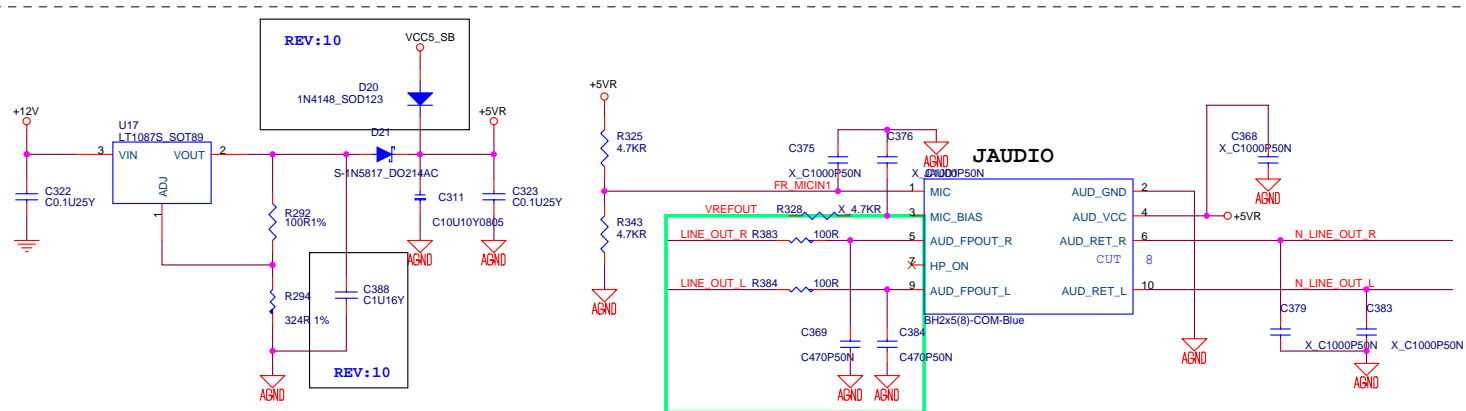
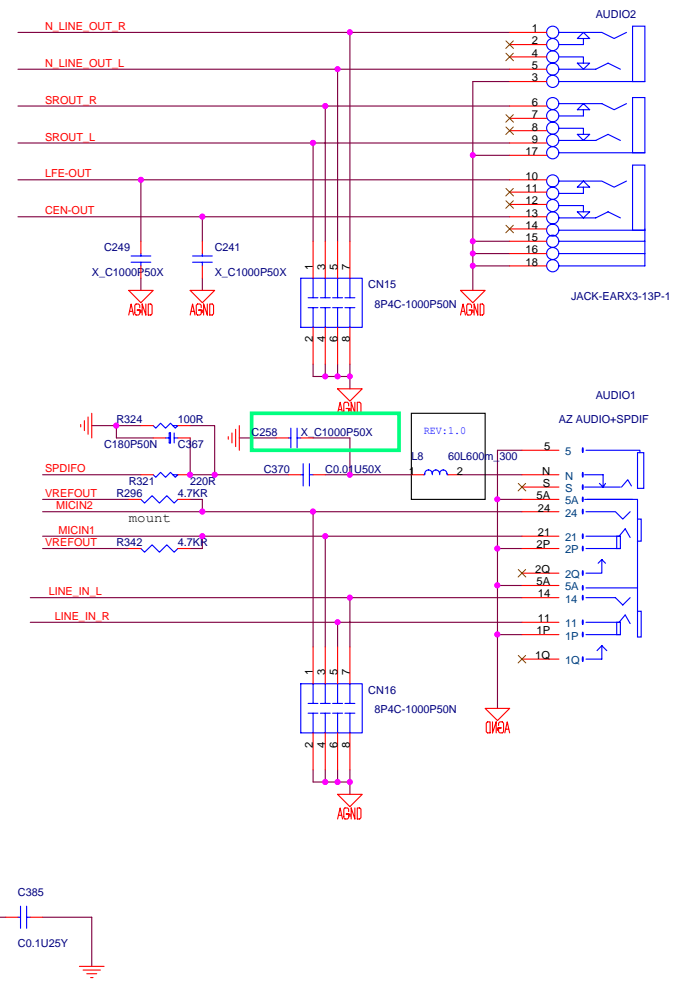
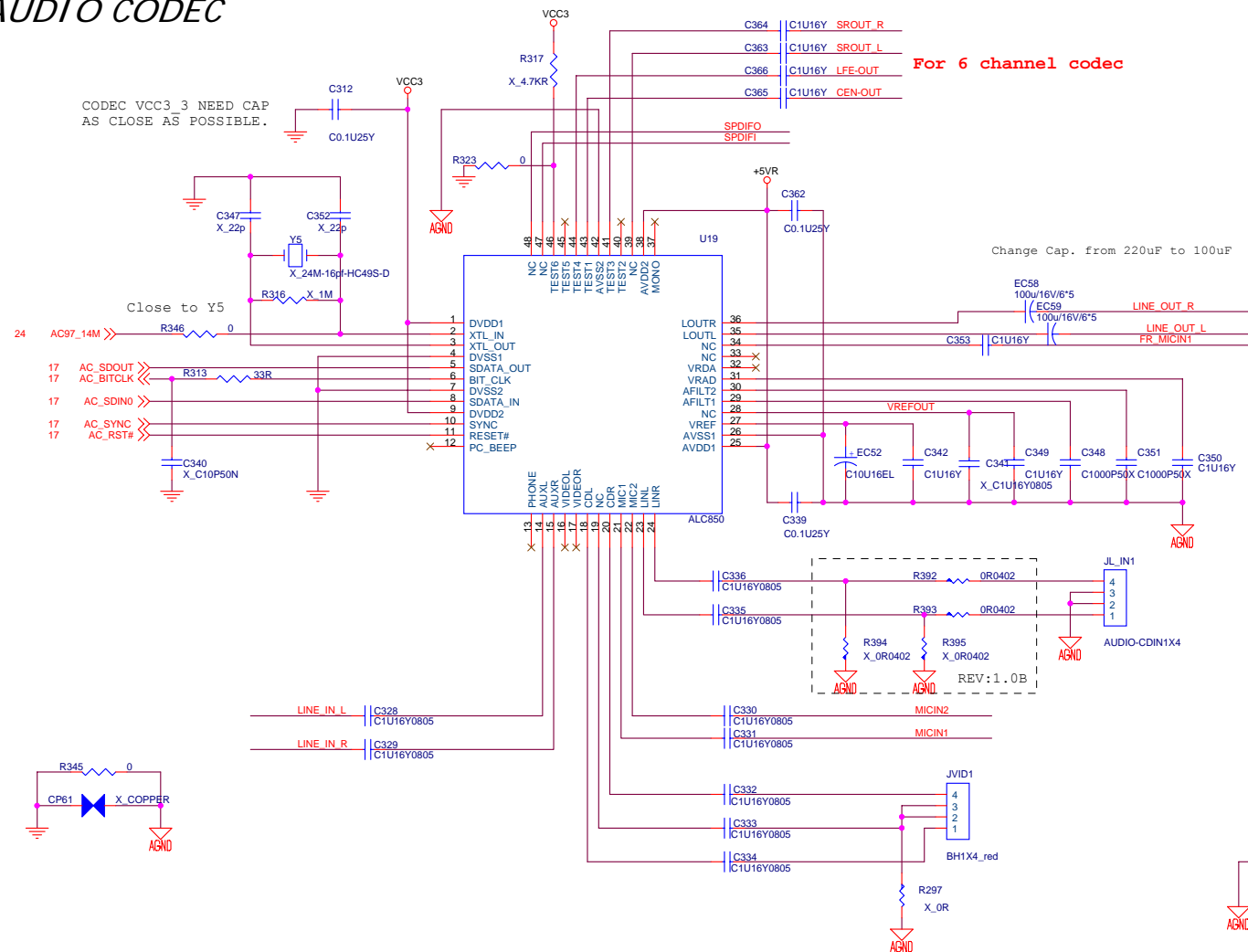
DDRVREF GEN. & DECOUPLING

change CP2 to bead



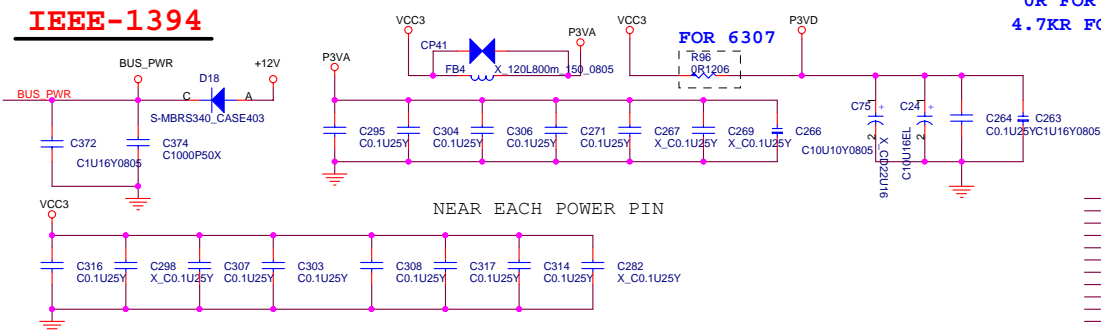
		MICRO-STAR	
Title Clock Buffer			
Size	Document Number MS-7233		Rev 10
Date:	Thursday, November 10, 2005	Sheet	25 of 36

AUDIO CODEC

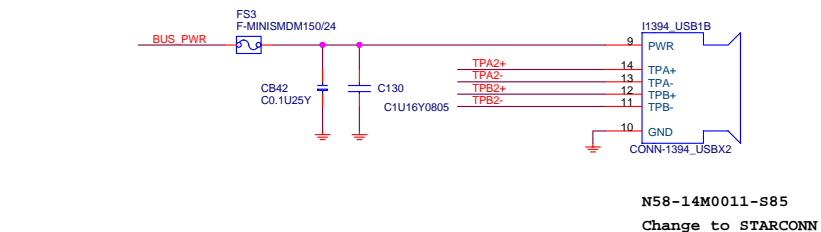
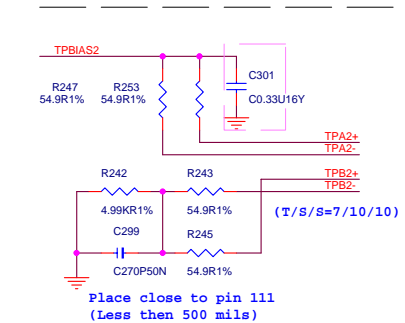
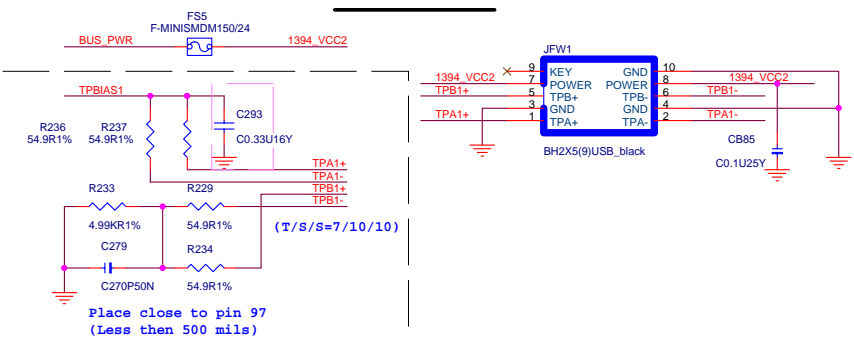




IEEE-1394

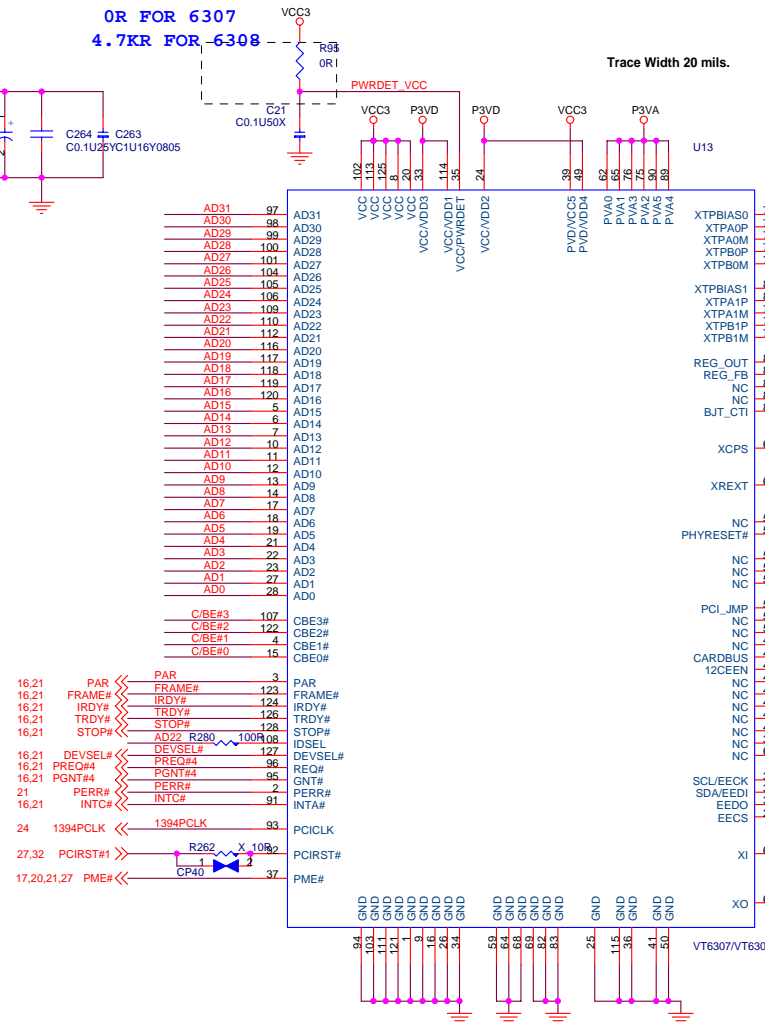


FRONT 1394 PORT 1



N58-14M0011-s85
Change to STARCONN

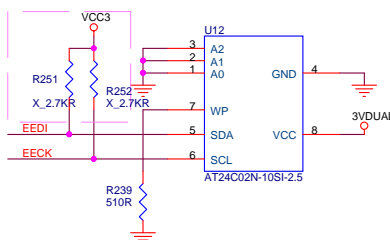
OR FOR 6307 4.7K FOR 6308



AD31	97	AD31	97
AD30	98	AD30	98
AD29	99	AD29	99
AD28	100	AD28	100
AD27	101	AD27	101
AD26	102	AD26	102
AD25	103	AD25	103
AD24	104	AD24	104
AD23	105	AD23	105
AD22	106	AD22	106
AD21	107	AD21	107
AD20	108	AD20	108
AD19	109	AD19	109
AD18	110	AD18	110
AD17	111	AD17	111
AD16	112	AD16	112
AD15	113	AD15	113
AD14	114	AD14	114
AD13	115	AD13	115
AD12	116	AD12	116
AD11	117	AD11	117
AD10	118	AD10	118
AD9	119	AD9	119
AD8	120	AD8	120
AD7	121	AD7	121
AD6	122	AD6	122
AD5	123	AD5	123
AD4	124	AD4	124
AD3	125	AD3	125
AD2	126	AD2	126
AD1	127	AD1	127
AD0	128	AD0	128

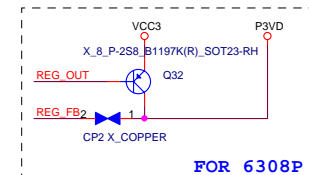
20040312
JuneWu@vntek.com.tw
suggestion modify

1394-EEPROM 24C02

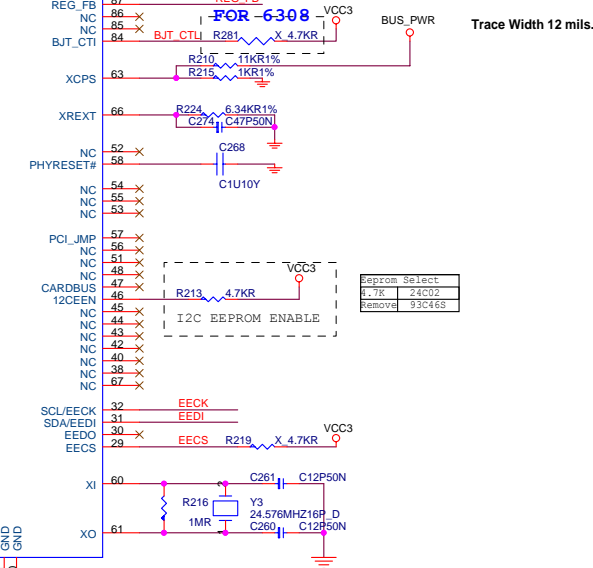


16.21 AD[0..31] << AD[0..31]
16.21 C/BE#[3..0] << C/BE#[3..0]

IDSEL AD22
MASTER = PREQ#4
INTD#



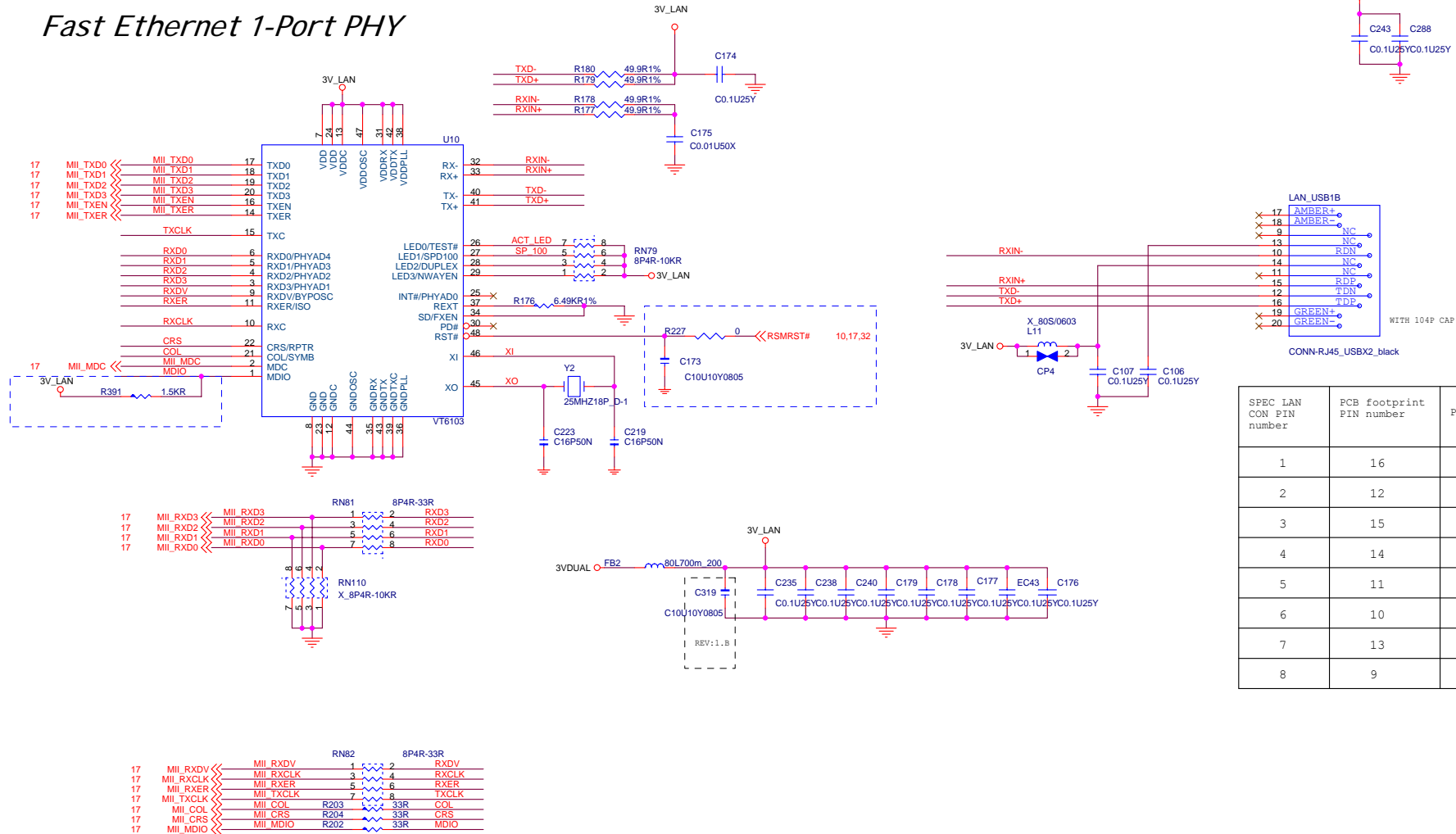
BJT_CTL
0: Internal power MOS
1: External BJT



IDSEL AD22
MASTER = PREQ#4
INTD#

MICRO-STAR	
Title	1394 - VIA VT-6307
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Fast Ethernet 1-Port PHY



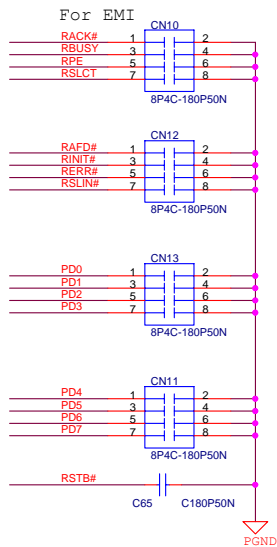
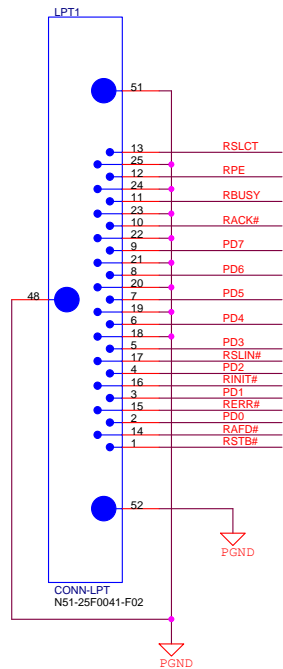
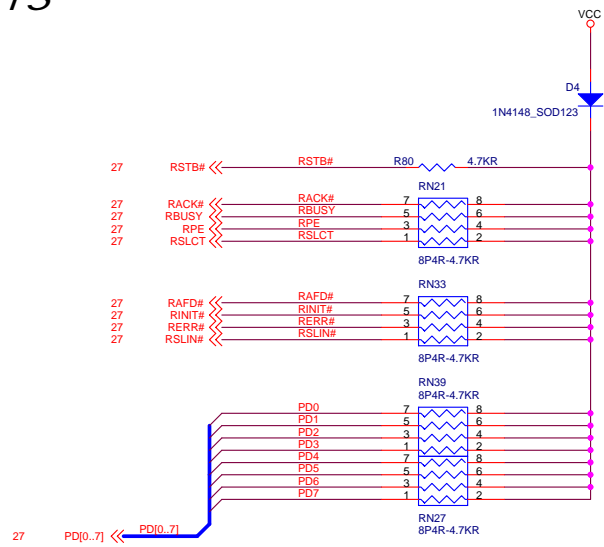
SPEC LAN CON PIN number	PCB footprint PIN number	PIN Define
1	16	TXD+
2	12	TXD-
3	15	RXIN+
4	14	TCT
5	11	NC
6	10	RXIN-
7	13	RCT
8	9	NC



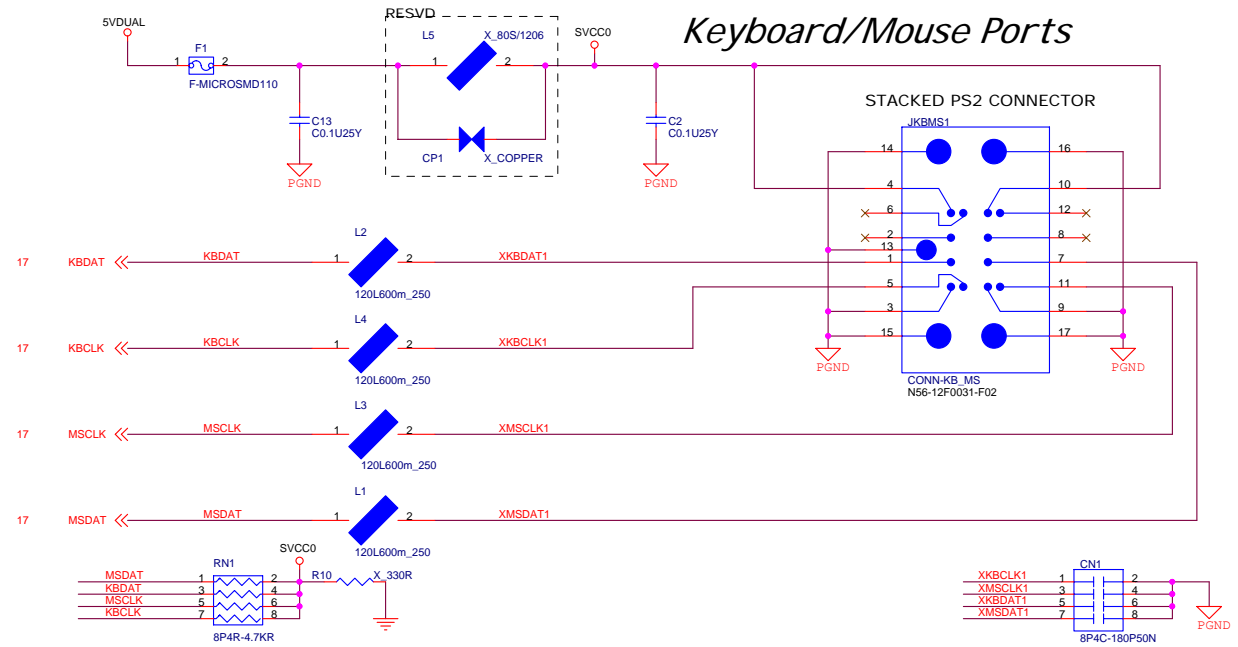
MICRO-STAR

Title	LAN	
Size	Document Number	Rev 1B
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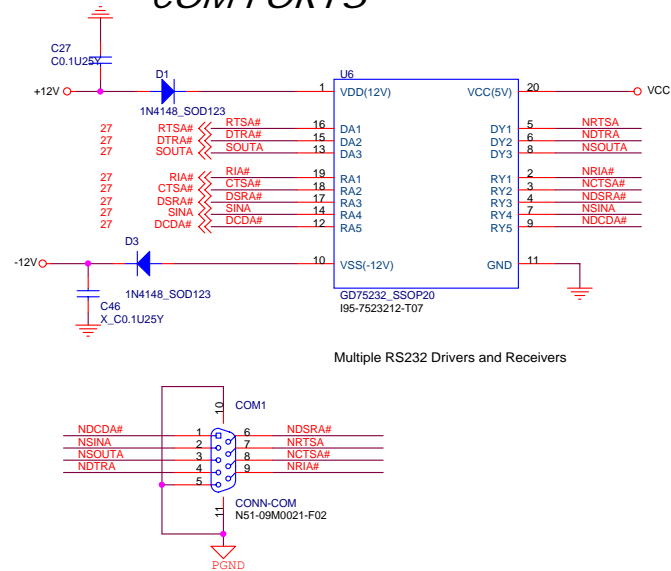
LPT PORTS



Keyboard/Mouse Ports

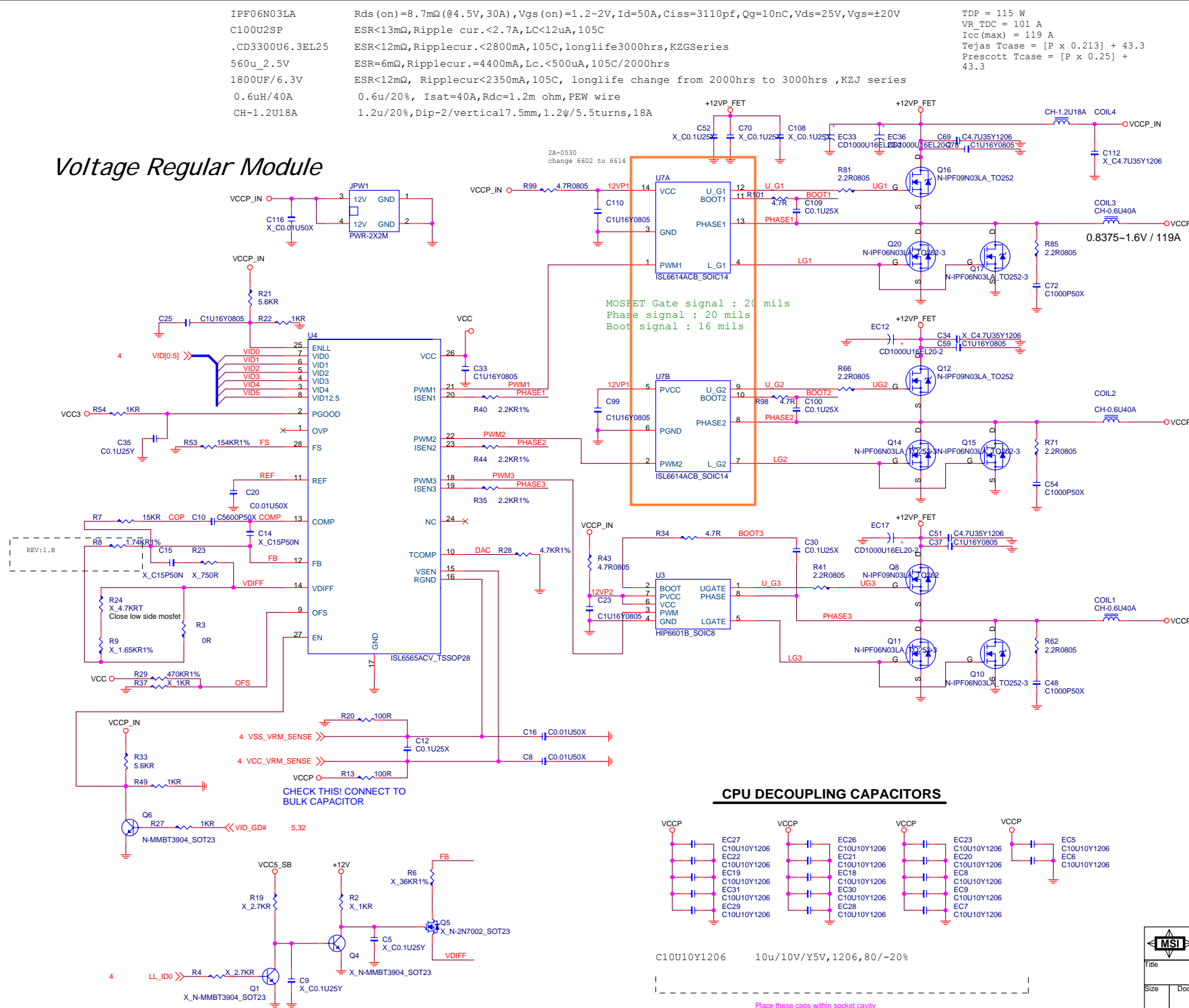


COM PORTS



		MICRO-STAR	
Title: LPT/COM PORT			
Size	Document Number		Rev 1B
		MS-7233	
Date:	Thursday, November 10, 2005	Sheet	30 of 36

Voltage Regular Module



ACPI Controller

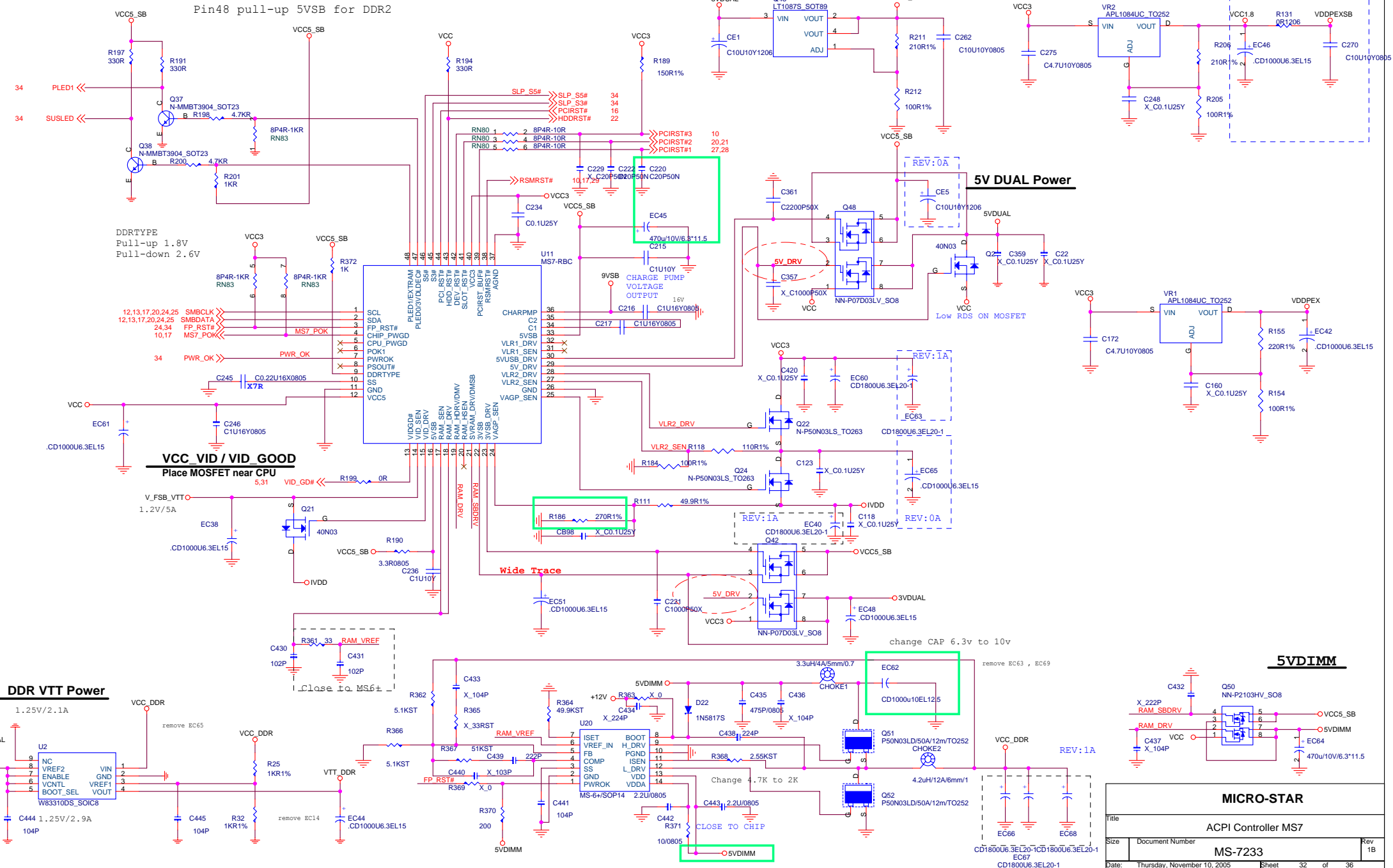
ICH5 300mA
PCI 375+20+20= 415mA
VCC3_SB 715mA

	S0	S3	S5
Power	Main	Standby	Standby
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	Standby
MEM_STR	Main	Standby	0V

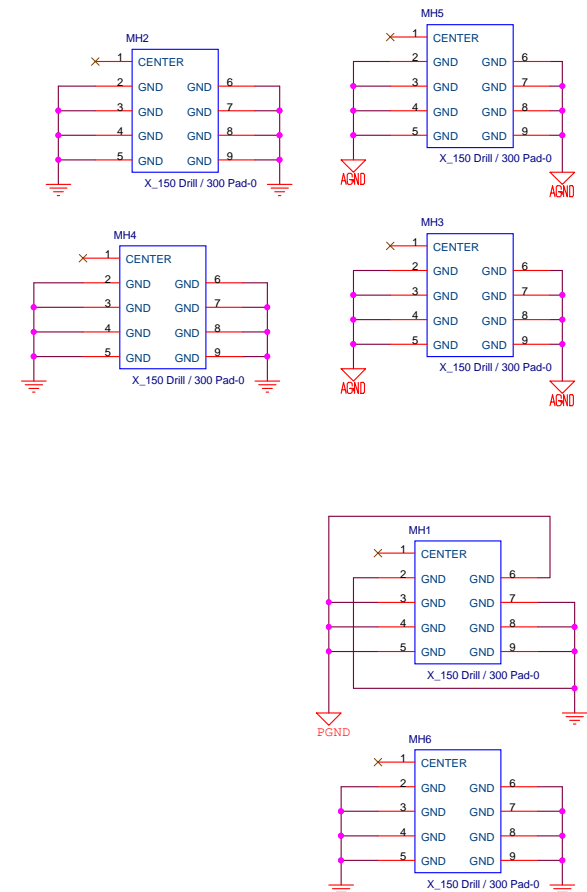
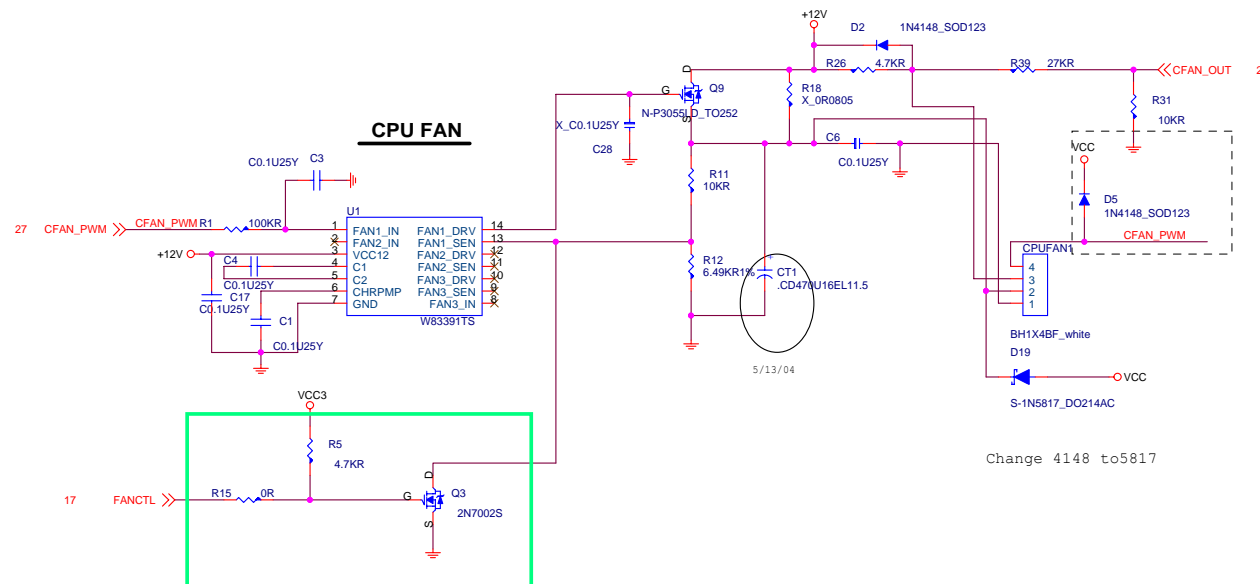
1.7V@250mA

1.8V STAND BY POWER

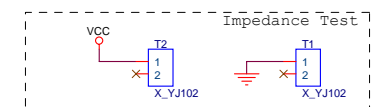
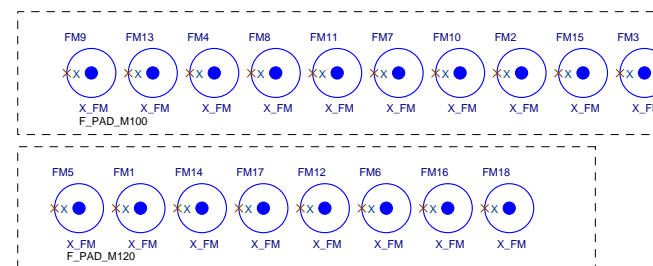
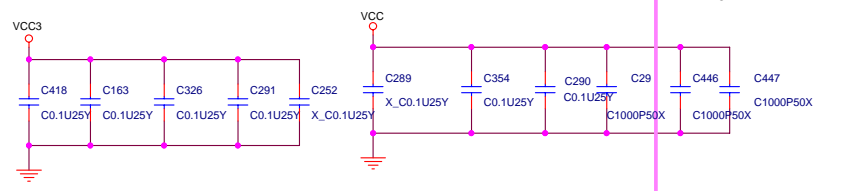
VDDPEXS W=25mils



ATX VIA-Hole * 9

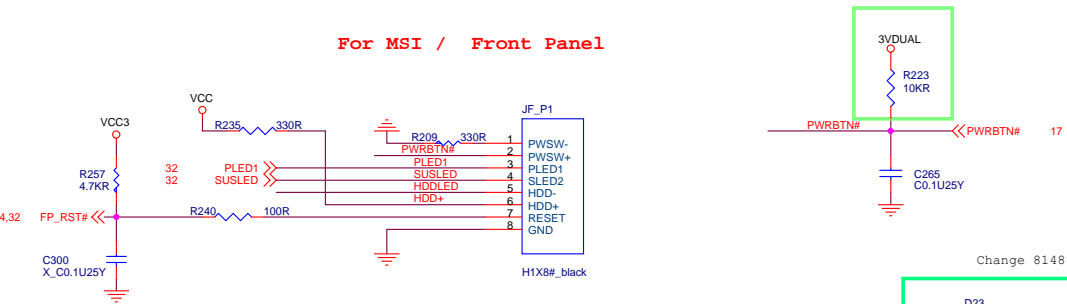


BULK / Decopuling

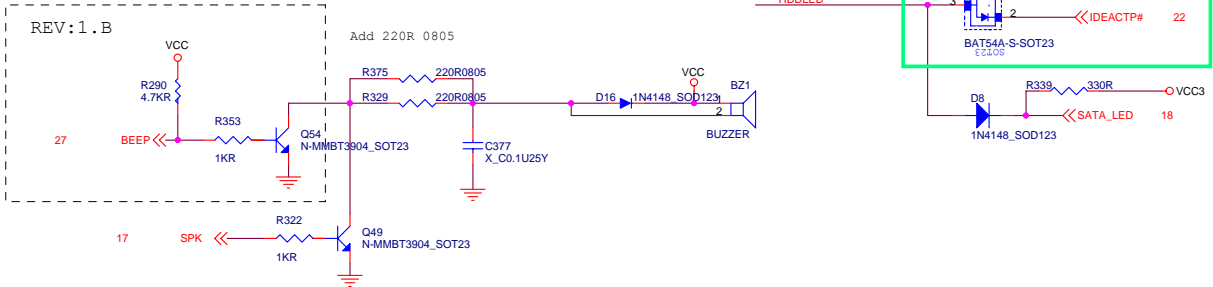
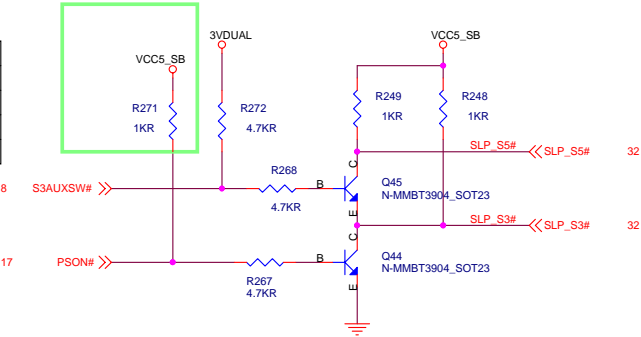


FRONT PANEL

For MSI / Front Panel



	S0	S3	S5
S3AUXSW#	1	0	1
PSON#	0	1	1
SLP_S5#	1	1	0
SLP_S3#	1	0	0



ATX Connector

